

Compal Confidential

FOC90/FOY50

ICL-U

M/B Schematics Document

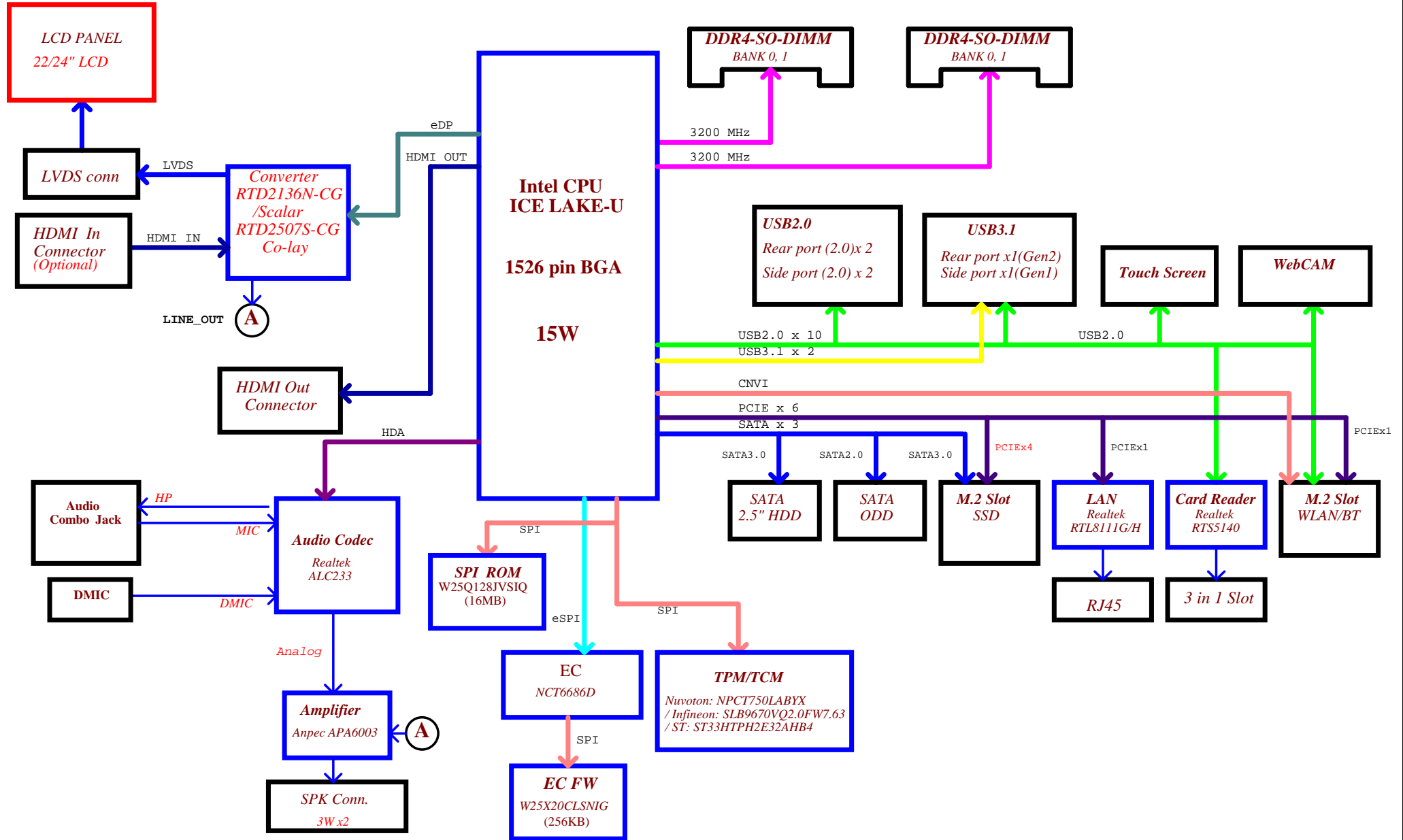
LA-K531P

2020-08-25

REV : 1.0

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			2019/2/5	Cover Page	
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Black Diagram



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PCIe Port Table		
No.	Port	Device
1	9	LAN
2	10	WLAN
3	13	SSD
4	14	SSD
5	15	SSD
6	16	SSD

SATA Port Table		
No.	Port	Device
1	11	HDD
2	12	ODD
3	15	SSD
4	16	SSD

DDI Port Table		
No.	Port	Device
1	DDIA	DP to LVDS CVT
2	DDIB	HDMI OUT

BOARD ID Table	
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0

USB2.0 Port Table		
Port	Device	OC# Pin
1	JUSB3 (Rear) USB3.1	OC1#
2	JUSB4 (Side) USB3.1	OC2#
3	JUSB1 (Rear) USB2.0	OC0#
4	JUSB2 (Rear) USB2.0	
5	Card Reader	NA
6	TOUCH	NA
7	Web Camera	NA
8	JUSB6 (Side) USB2.0	OC3#
9	JUSB5 (Side) USB2.0	
10	WLAN/BT	NA

USB3.0 Port Table		
No.	Port	Device
1	1	USB3.0 (Rear IO) GEN2
2	2	NC
3	3	NC
4	4	USB3.0 (Side IO) GEN2
5	5	NC
6	6	NC

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+20VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+RTCVCC_S5	RTC power	ON	ON	ON*
+3V3_DS_W	3.3V DS_W on power rail	ON	ON	ON*
+3VALW_S5	3.3V always on power rail	ON	ON	ON
+5VALW_S5	5V always on power rail	ON	ON	ON
+12VS_S0	12V power rail	ON	ON*	ON*
+1.8VALW_S5	1.8V always on power rail	ON	ON	ON
+1.8V_PRIM_S0	1.8V PRIM power rail for PCH	ON	OFF*	OFF*
+1.05V_VCCST_S3	1.05V power rail for CPU VCCST	ON	ON	OFF*
+1.2V_VDDQ_S3	1.2V power rail for DDR4	ON	ON	OFF*
+2.5V_S3	2.5V power rail for DDR4	ON	ON	OFF
+1.05VS_VCCSTG_S0	1.05V power rail for CPU VCCSTG	ON	ON	OFF*
+5VS_S0	5V switched power rail	ON	OFF	OFF
+3VS_S0	3.3V switched power rail	ON	OFF	OFF
+VCCIN	VCC Core voltage for CPU	ON	OFF	OFF
+VCCIN_AUX	Core voltage for CPU graphic	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.
Note : 12VS_S0 S3/S5 ON only for S0IX-IN function need.
Note : +1.8V_PRIM_S0 , S3/S5 OFF only for S0IX function enable
Note : +1.05V_VCCSTG_S3 , S5 OFF only for premium power design
Note : +1.05VS_VCCSTG_S0 , S5 OFF only for premium power design

SKU ID(Project) Table

SKU (UMA&DIS)	A350-FOC90 IIL SIT BOM Configure Table
451AO938L31	F@S@T/WITM/AS@NB@P@SMR@DV@PL@ /310G@
431AO938L31	
Converter	
X4EAO938L31	M@FB@R@
451AO938L32	F@S@T/WITM/AS@NB@P@SMR@DF@N@ /F10G@
431AO938L32	
Converter	
X4EAO938L31	M@FB@R@
451AO938L33	F@S@T/WITM/AS@NB@P@SMR@DF@N@ /710G@
431AO938L33	
Converter	
X4EAO938L31	M@FB@R@

SKU (UMA&DIS)	V30a-FOY50 IIL SIT BOM Configure Table
451AO938L01	F@S@T/WITM/AS@NB@P@SMR@DV@PL@ /310G@
431AO938L01	
SCALAR	
X4EAO938L01	M@FB@R@
451AO938L02	F@S@T/WITM/AS@NB@P@SMR@DF@N@ /510G@
431AO938L02	
SCALAR	
X4EAO938L01	M@FB@R@

BOM Structure	BTO Item
F@S@T/WITM/AS@NB@P@SMR@DV@PL@ /310G@	AKS1888P2
U@P@	U@P@
F@S@T/WITM/AS@NB@P@SMR@DV@PL@ /310G@	F@S@T/WITM/AS@NB@P@SMR@DV@PL@ /310G@
CH@P@T@C@T@B@Y@M	CH@P@T@C@T@B@Y@M
M@I@P@M@B@T	M@I@P@M@B@T
E@D@P@M@B@T	E@D@P@M@B@T
G@R@P@M@B@T	G@R@P@M@B@T
G@A@O@B@T@Y	G@A@O@B@T@Y
G@V@A@B@T@Y	G@V@A@B@T@Y
M@I@P@M@B@T	M@I@P@M@B@T
E@D@P@M@B@T	E@D@P@M@B@T
D@T@L@C@T@B@Y@M	D@T@L@C@T@B@Y@M
S@E@A@H@D@I@N	S@E@A@H@D@I@N
E@P@R@d@H@M@I@N@E@I@P@M@B@T	E@P@R@d@H@M@I@N@E@I@P@M@B@T
S@E@A@H@D@I@N@E@I@P@M@B@T	S@E@A@H@D@I@N@E@I@P@M@B@T
R@E@P@R@d@I@B@g	R@E@P@R@d@I@B@g
G@W@N@7@B@g	G@W@N@7@B@g
B@E@W@N@d@B@g	B@E@W@N@d@B@g
H@I@M	H@I@M
O@H@I@M	O@H@I@M
F@R@S@I@M	F@R@S@I@M
G@I@H@P@N@I@M	G@I@H@P@N@I@M
G@N@U@P@N@I@M	G@N@U@P@N@I@M
G@M@B@N@S@B@g	G@M@B@N@S@B@g
B@E@M@A@P@S@H@B	B@E@M@A@P@S@H@B
G@C@N@I@P@H@T@C@B@P@H@	G@C@N@I@P@H@T@C@B@P@H@
O@V@I@T@E@N@P@M@B@T	O@V@I@T@E@N@P@M@B@T
F@S@K@T@P@W@R@O	F@S@K@T@P@W@R@O
G@S@M@R@P@O@E@O@N	G@S@M@R@P@O@E@O@N

PCH SM Bus Address

Device	Address	HEX
DDR(JDIMM1)	WRITE:0xA0	READ: 0xA1
DDR(JDIMM2)	WRITE:0xA4	READ: 0xA5

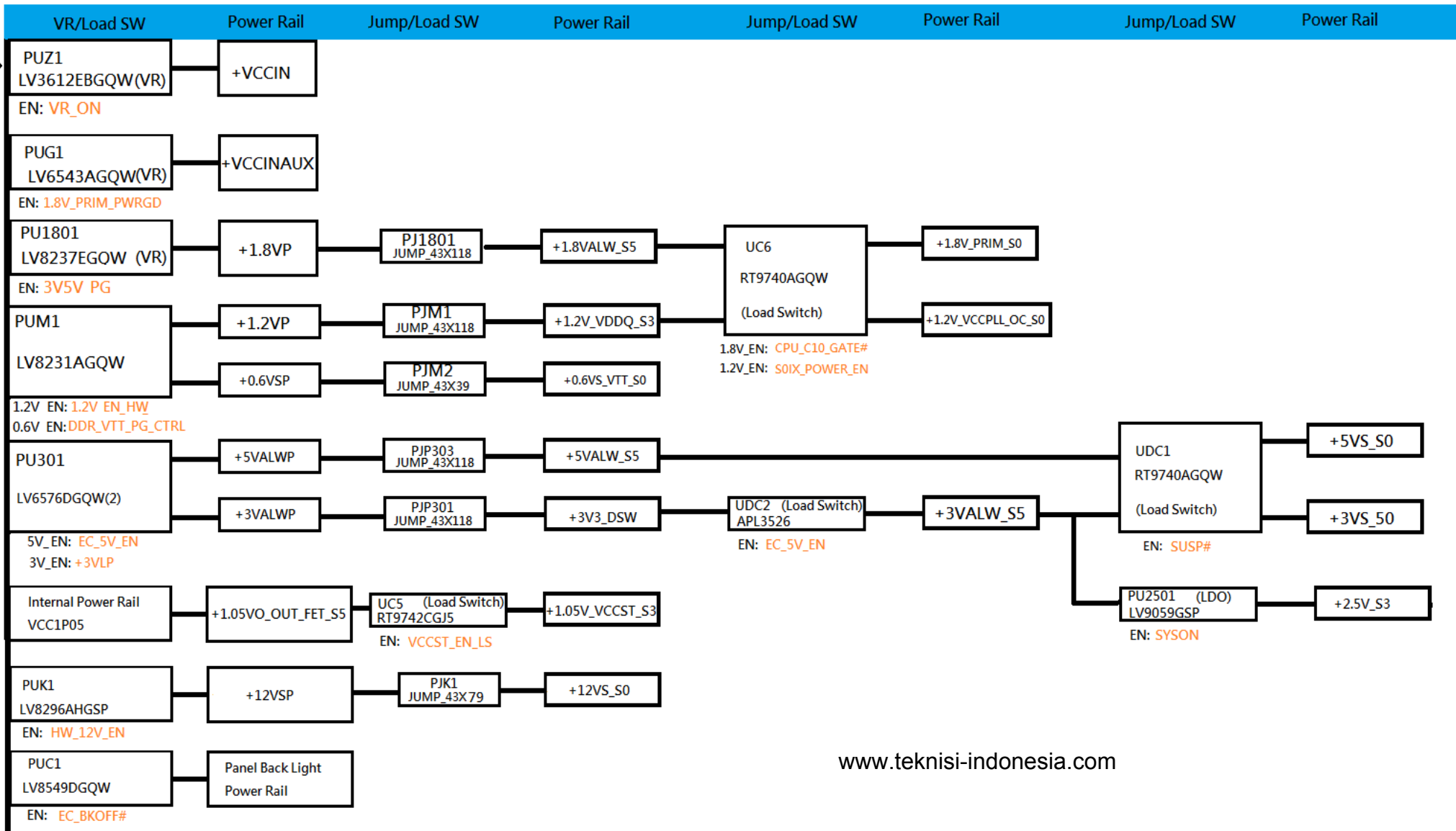
EC SM Bus0 Address

Device	Address	HEX
PCH	1001-0000xb	90
Thermal	1001-1010xb	9A

EC SM Bus2 Address

Device	Address	HEX
LCD Backlight	0110-0010xb	62
Converter RTD-2136N / RTD2507S	1001-0100xb	94

+20VB



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G3->S0

S0-> S0ix

S0ix ->S0

S0->S5

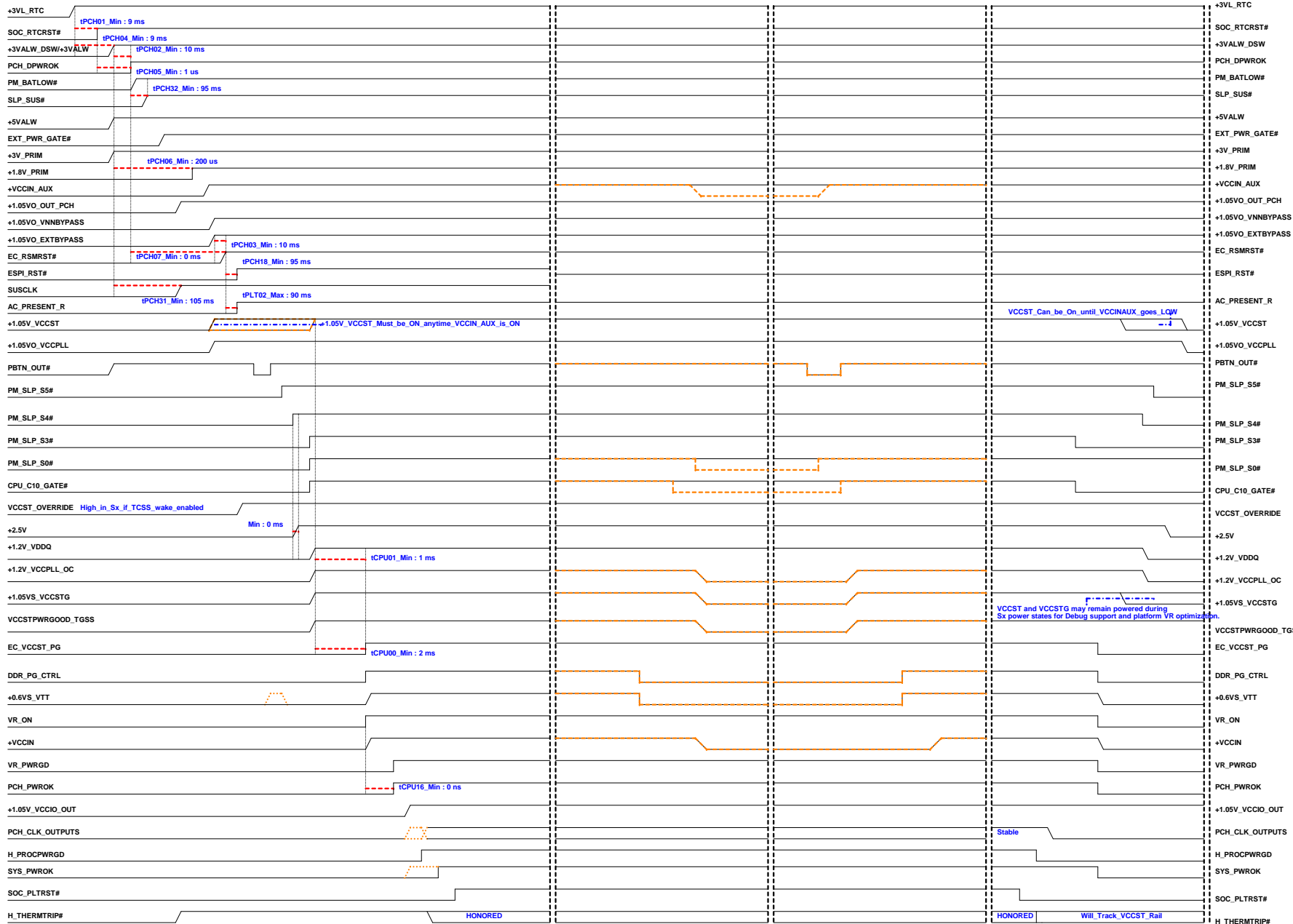
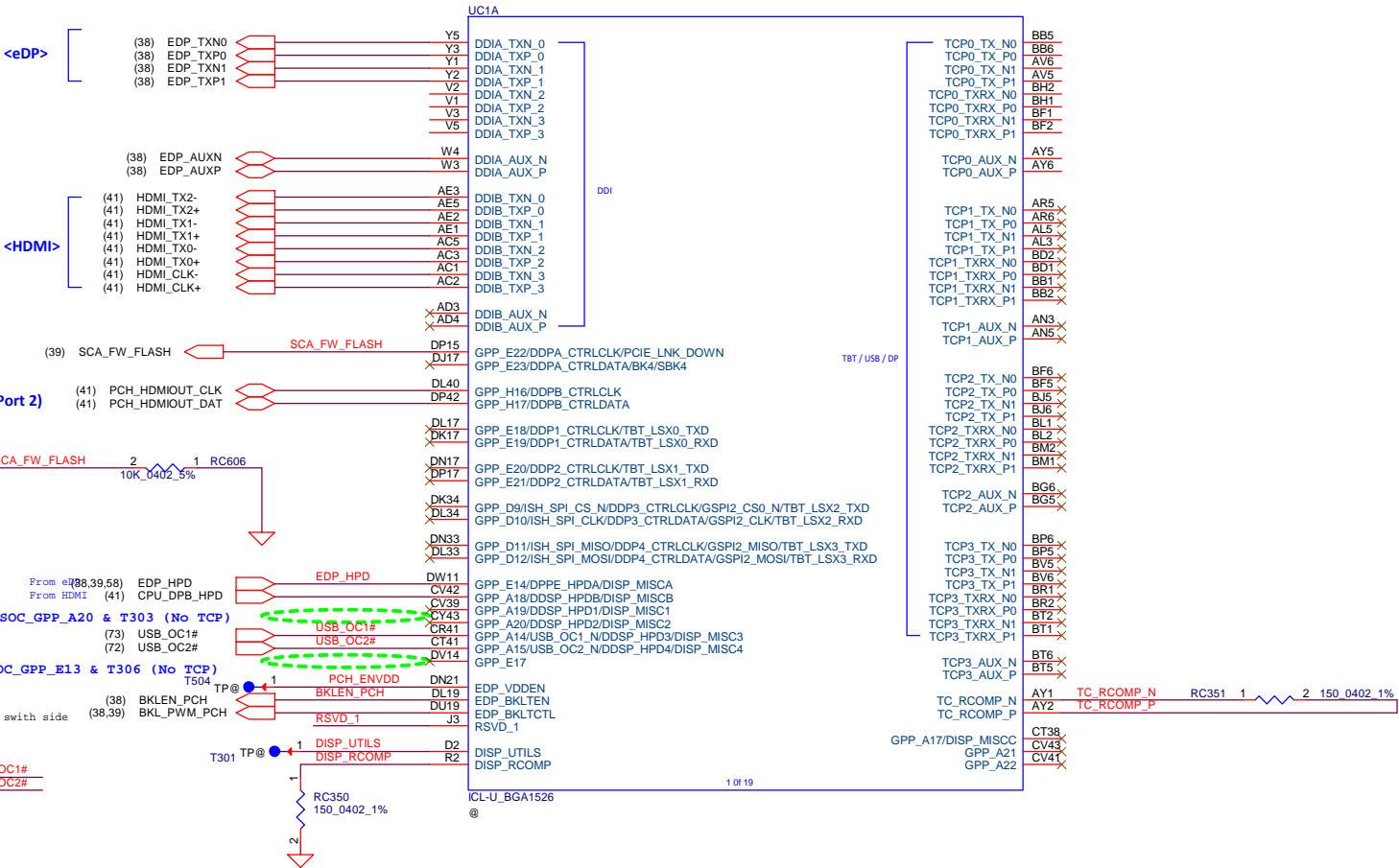


Table 7-1. Mapping of HDMI* Signals for DDI Ports

Port	Digital Display Interface Pins	CRB Digital Display Interface Signals	HDMI* Signals
Port 1	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIx_TX2_DP
	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIx_TX2_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIx_TX1_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIx_TX1_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIx_TX0_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIx_TX0_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIx_CLK_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIx_CLK_DN
	Hot plug detect used by HDMI Port 1	DDPB_HPD	DDI1_HPD_Q
	HDMI DDC lines for Port 1	DDPB_CTRLCLK	DDI1_CTRL_CLK
	DDPB_CTRLDATA	DDI1_CTRL_DATA	



20200423 Add CPU UC1 BOM Structure

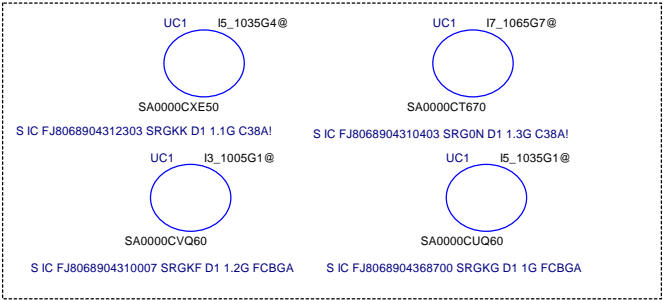


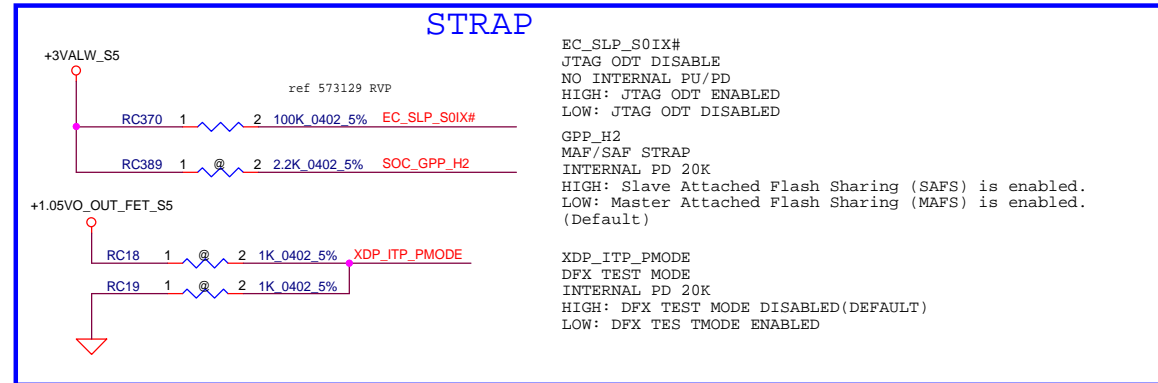
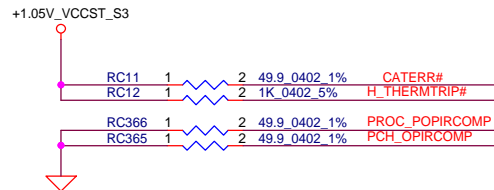
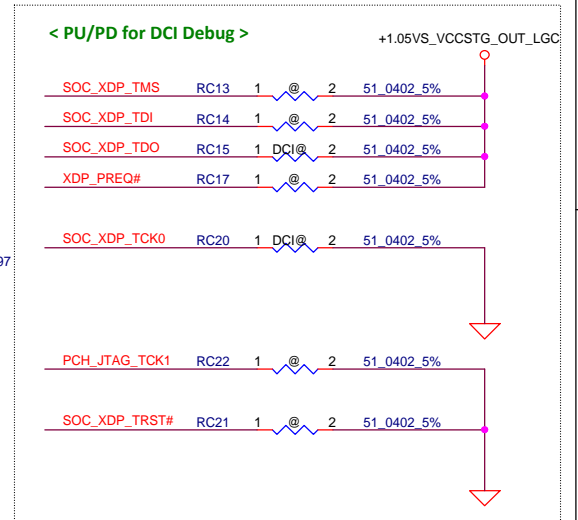
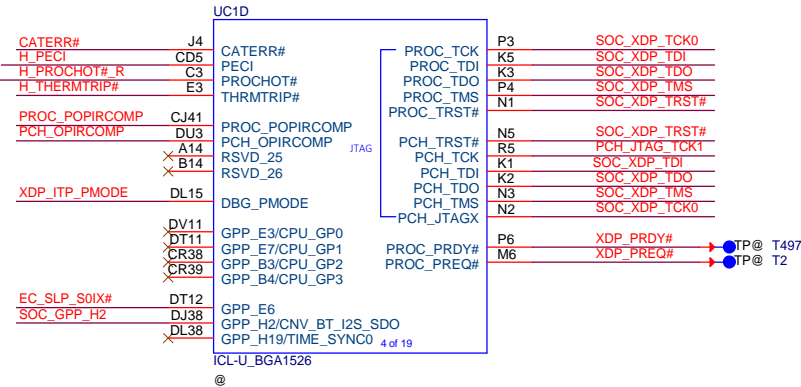
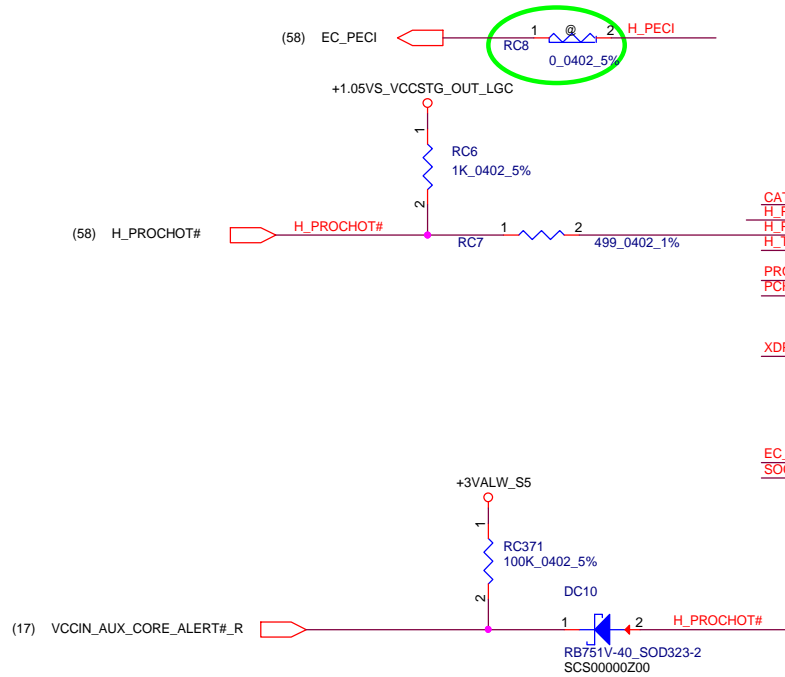
Table 5-11. USB3/USB2 Port Pairing for USB Type-C Connectors

	Connector C0	Connector C1	Connector C2	Connector C3
CPU USB3 port#	1	2	3	4
PCH USB2 port#	2	3	4	6

To make split xDCI controller working functionally for different USB-C connectors with increasing port numbers (TCP0_*, TCP1_*, TCP2_*, TCP3_*), recommended to pair with increasing number of USB2 ports from PCH. Simplest form of requirement is to match USB2/USB3 port numbers for USB-C connectors, but it is not strictly required.

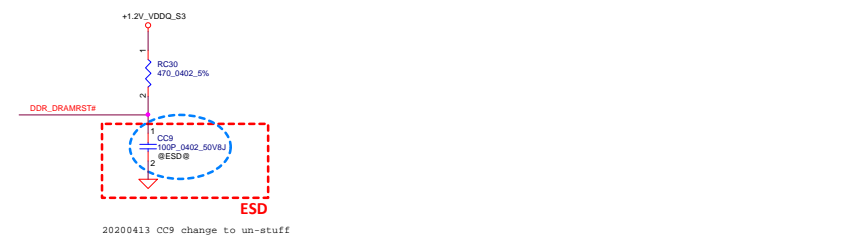
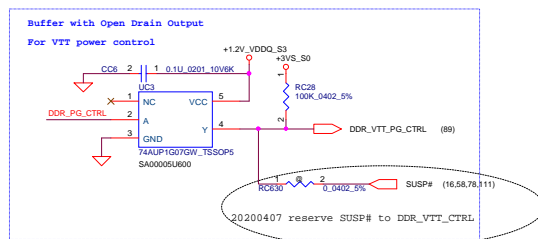
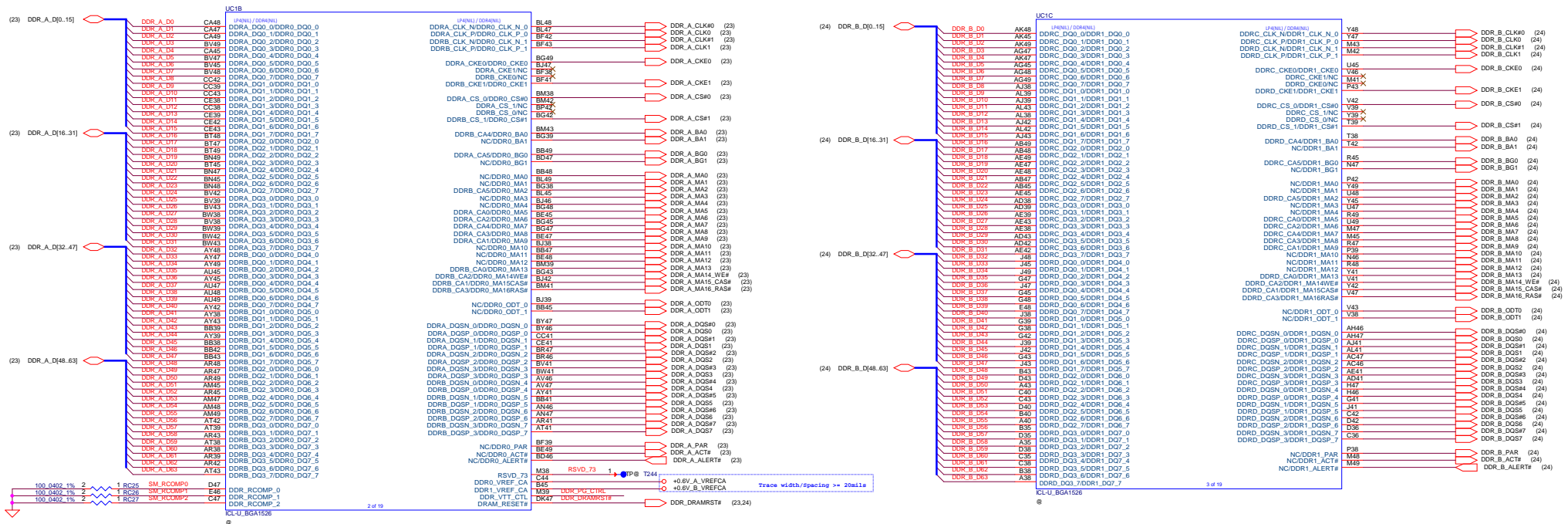
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20200807 RC8 -> R-SHORT

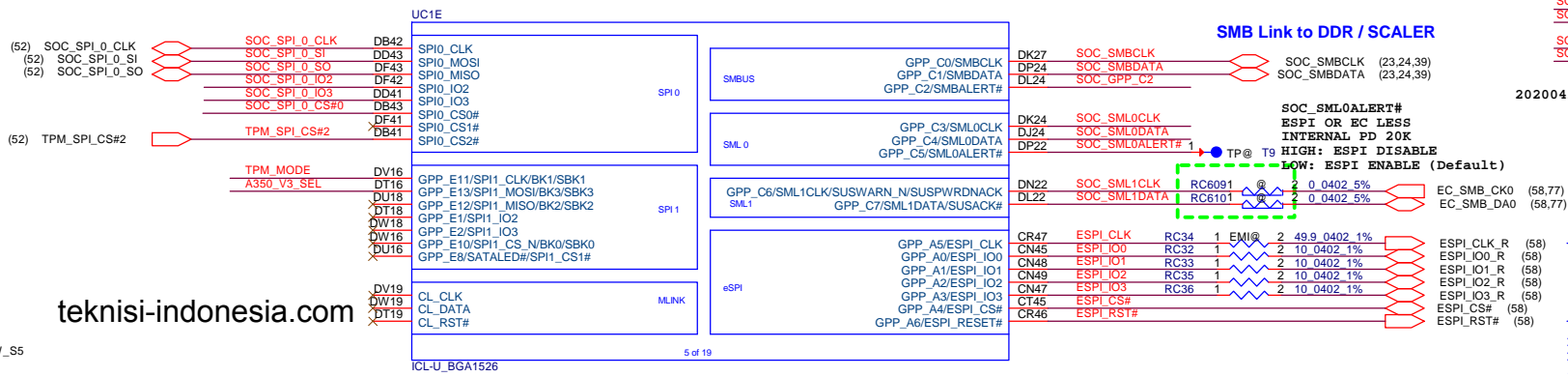


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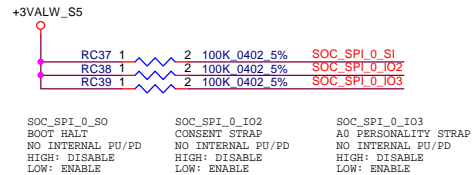
DDR4: Refer to 575034_ICL_U42_DDR4_T3_6L_Core_Schematics_Rev0p7



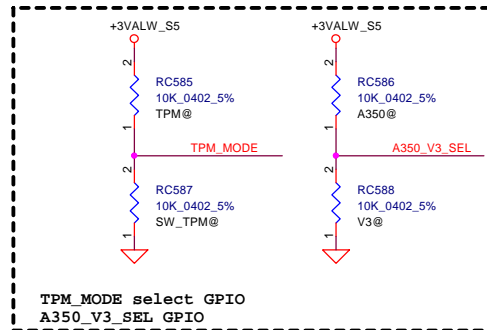
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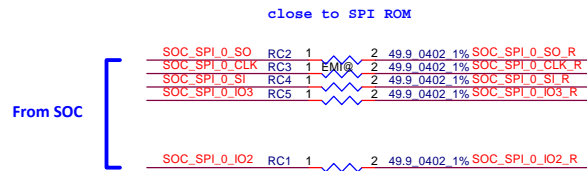
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_I02	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_I03	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



20200421 Remove SUSACK/SUSWARN

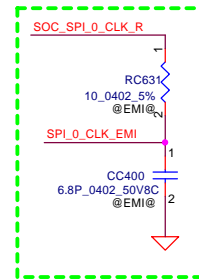
SUSWARN#/
 SUSPWRDNACK/

Will be eSPI Virtual Wire and no hard signal.

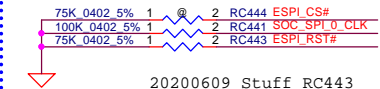


20200413 reserve RC Termination on SOC_SPI_0_CLK_R

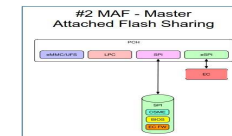
20200409 Add SPI ROM Socket co-layout
 20200413 Correct net name



20200807 Remove co-layout ROM Connect

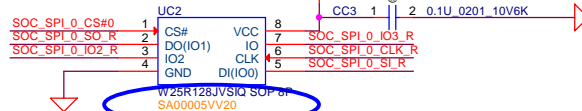


Follow 572907_ICL_UY_PDG for Glitch

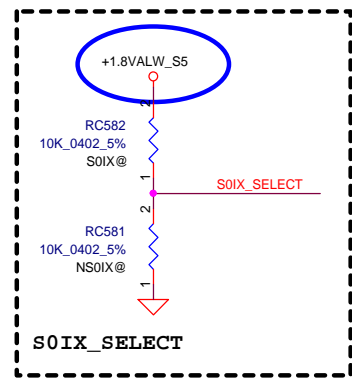


MAF - Master Attached Flash
 Single SPI Flash attached to SPI Bus
 EC FW access through eSPI Bus

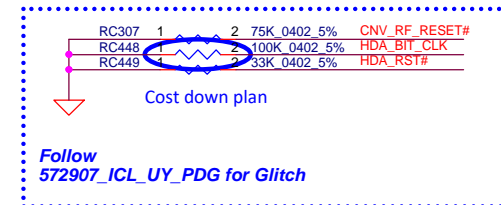
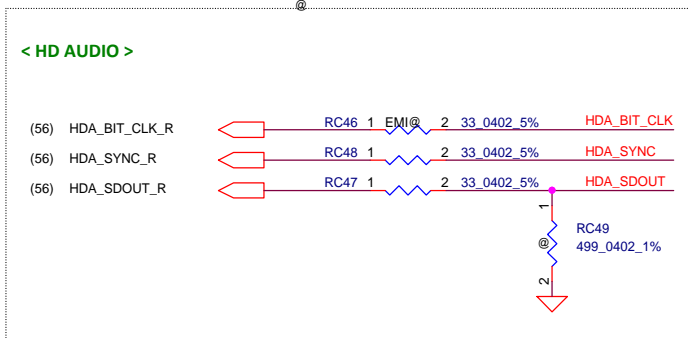
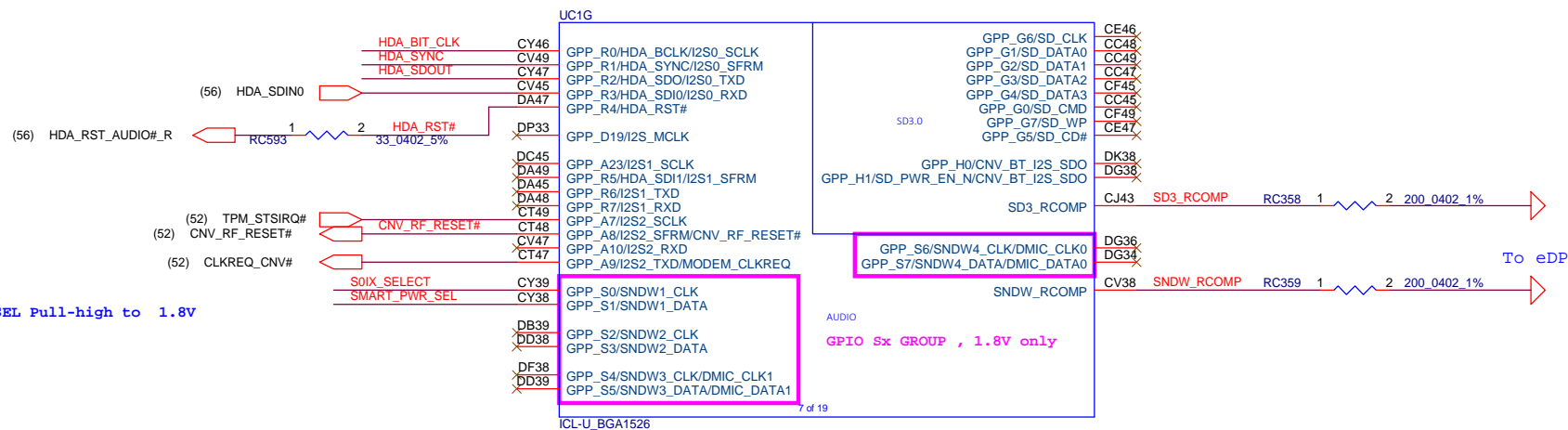
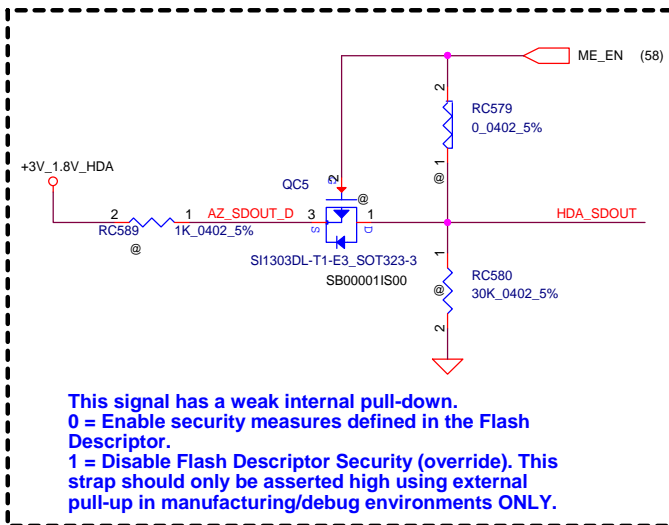
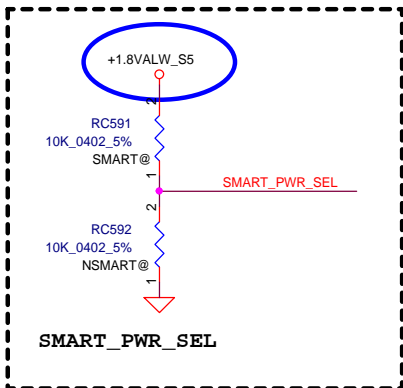
< SPI ROM - 16M >



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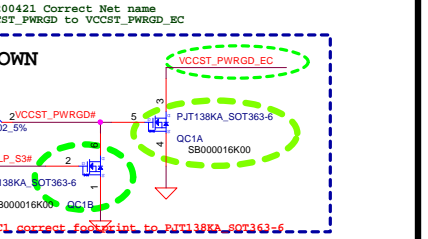
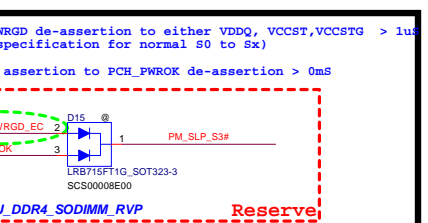
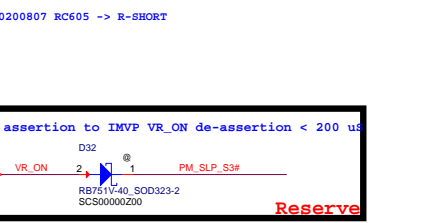
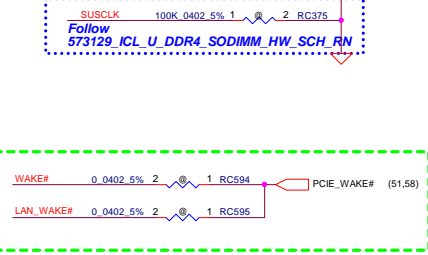
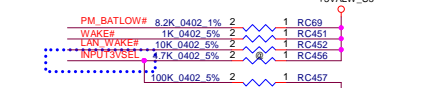
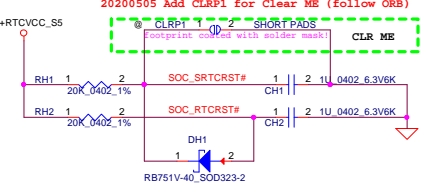
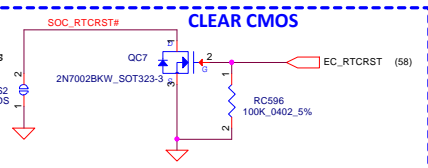
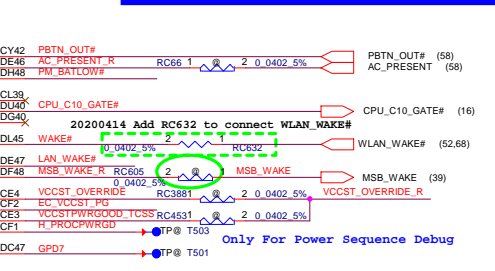
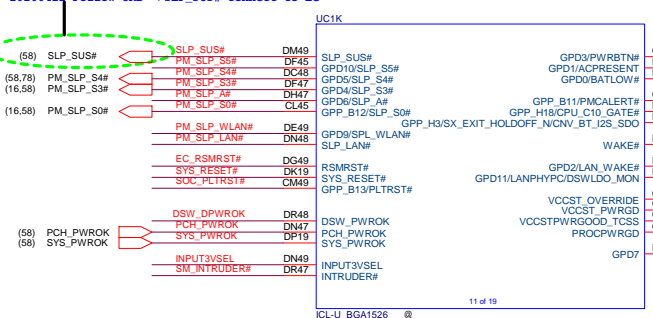
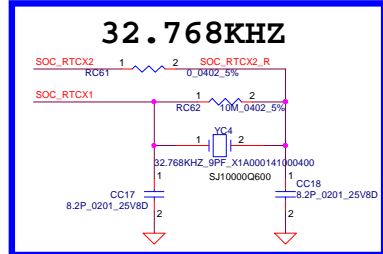
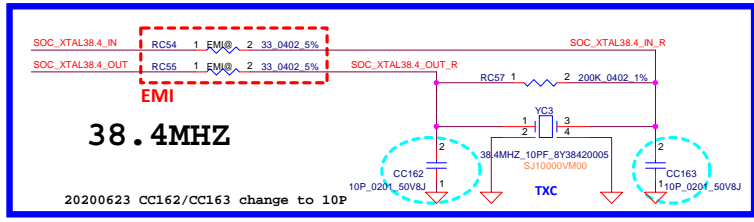
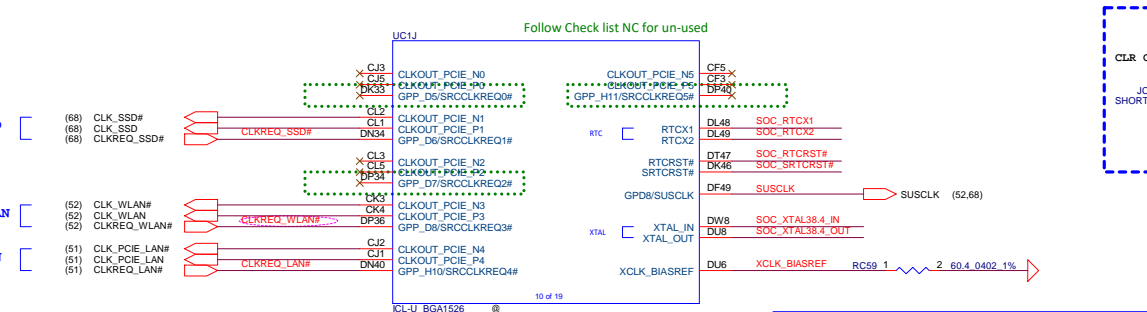
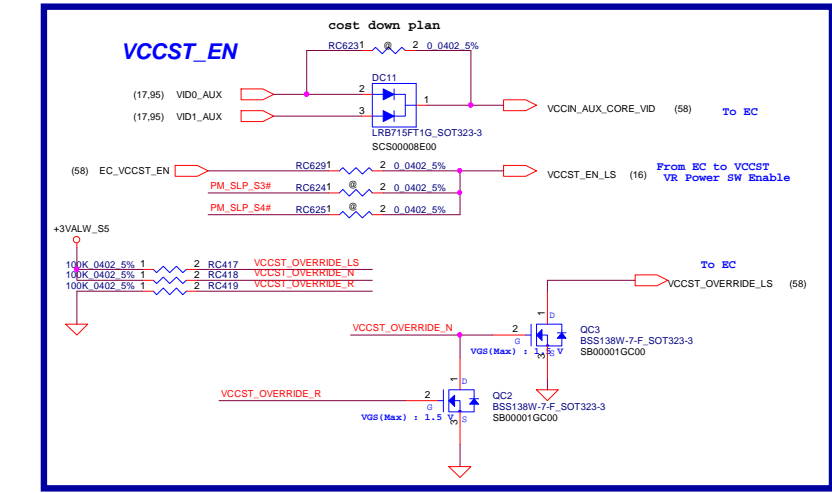
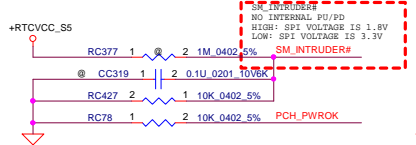
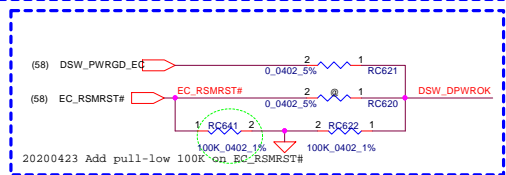
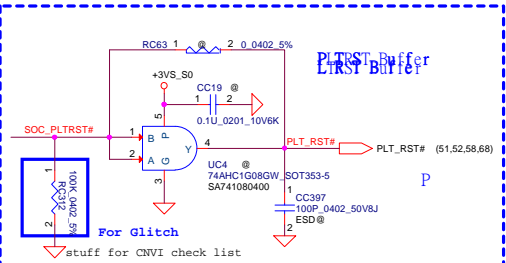
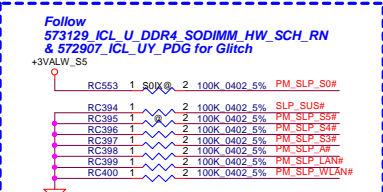
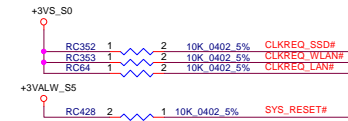


20200630 Correct SOIX_SELECT & SMART_PWR_SEL Pull-high to 1.8V

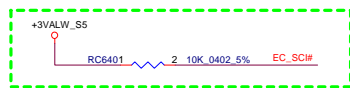


Follow 572907_ICL_UY_PDG for Glitch

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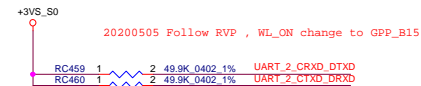


	Singal Name	Input
Premium	VCCIN_AUX_CORE_VID	H D D D L
	VCCST_OVERRIDE_LS	D H D D L
	PM_SLP_S3# (SUSP#)	D D H H L
	EC_VCCST_EN	Output H H H H L
	VCCIN_AUX_CORE_VID	H D D D L
Volume	VCCST_OVERRIDE_LS	D H D D L
	PM_SLP_S4# (SYSON)	D D D H L
	EC_VCCST_EN	Output H H H H L
	EC_VCCST_EN	Output H H H H L

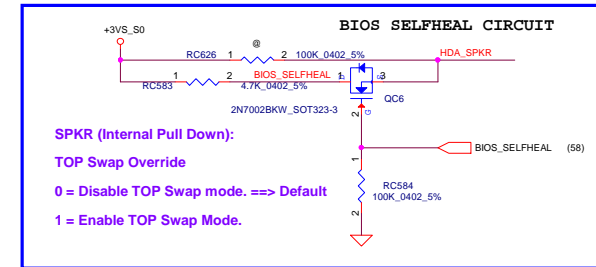
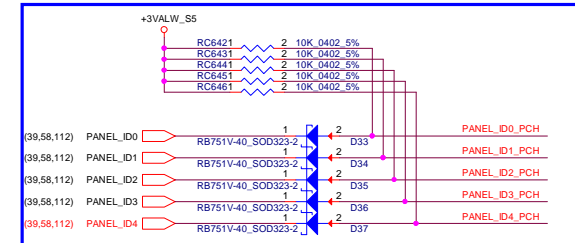


20200421 Remove RC614 (USB Side have PU already)

20200421 Add EC_SC1# pull-high 10K (+3VALW_S5)
20200505 Follow RVP, Add SOC_GPP_B18 for BT_Disable option.



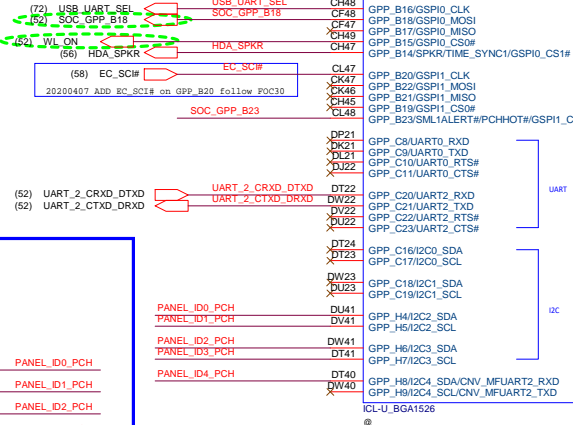
20200413 del unuse pull-high



(52) UART_2_CRXD_DTxD
(52) UART_2_CTxD_DRxD

PANEL_ID0_PCH
PANEL_ID1_PCH
PANEL_ID2_PCH
PANEL_ID3_PCH
PANEL_ID4_PCH

20200428 Add PANEL_ID0-4 SOC_GPIO

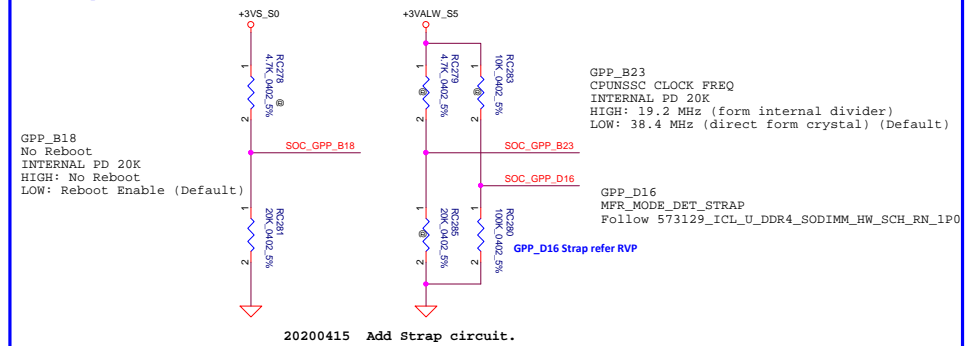


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20200413 Remove dGPU_Present net.

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Strap Pin



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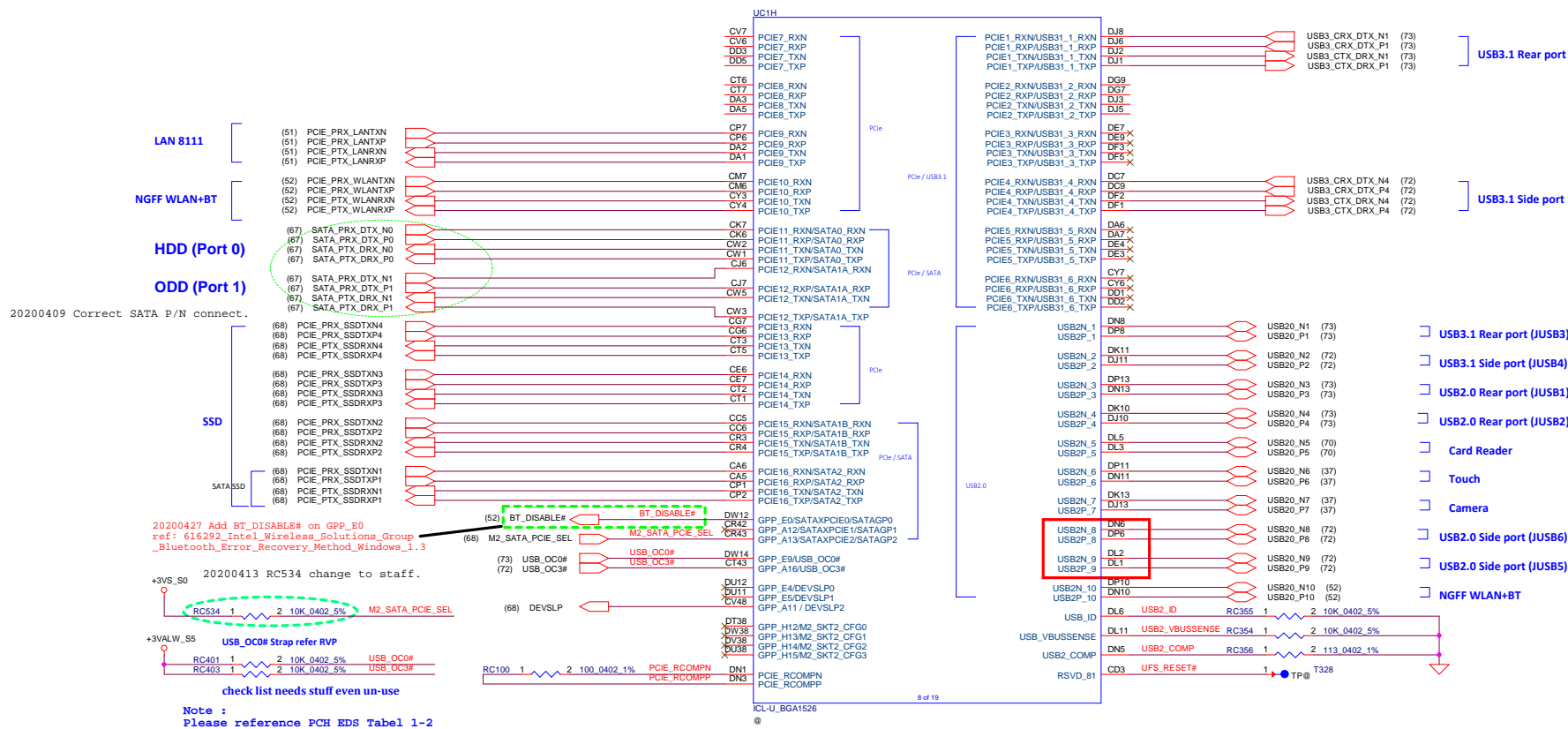


Table 1-2. PCH HSIO Details

Flex I/O Lane	SKU		
	Premium U	Premium Y	Base U
0	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1
1	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1
2	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1
3	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1
4	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1/Gen2, PCIe*	PCIe*
5	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1/Gen2, PCIe*	PCIe*
6	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
7	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
8	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
9	PCIe*	PCIe*	PCIe*
10	PCIe*, SATA	PCIe*, SATA	PCIe*, SATA
11	PCIe*, SATA	PCIe*, SATA	PCIe*, SATA
12	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
13	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
14	PCIe*, SATA	NA	PCIe*
15	PCIe*, SATA	NA	PCIe*

Table 6-24. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

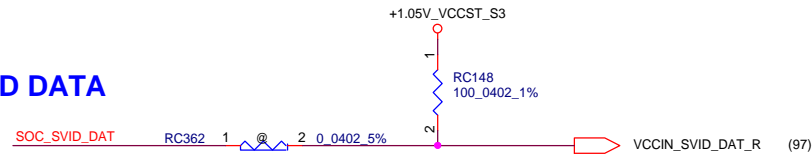
Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2 / SATA	PCI Express* Gen 3 / SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ¹	None ²	None ³

Notes:

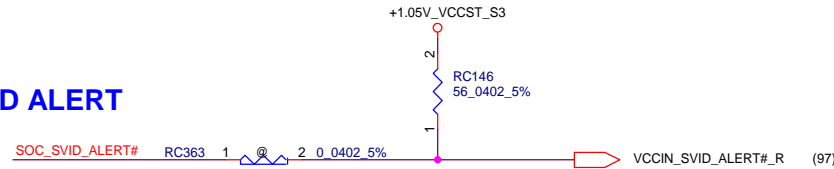
- This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / Devices are NOT used.
- For PCIe* Gen 2 / SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- For PCIe* Gen 3 / SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3 / SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

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SVID DATA



SVID ALERT



SVID CLOCK



5.5.10 SVID Topology

Figure 5-54. Routing Illustration for SVID Topology

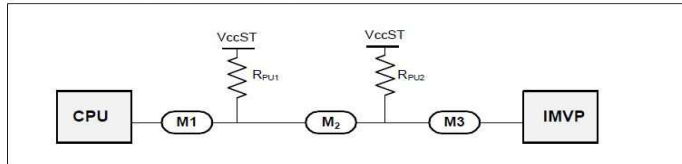
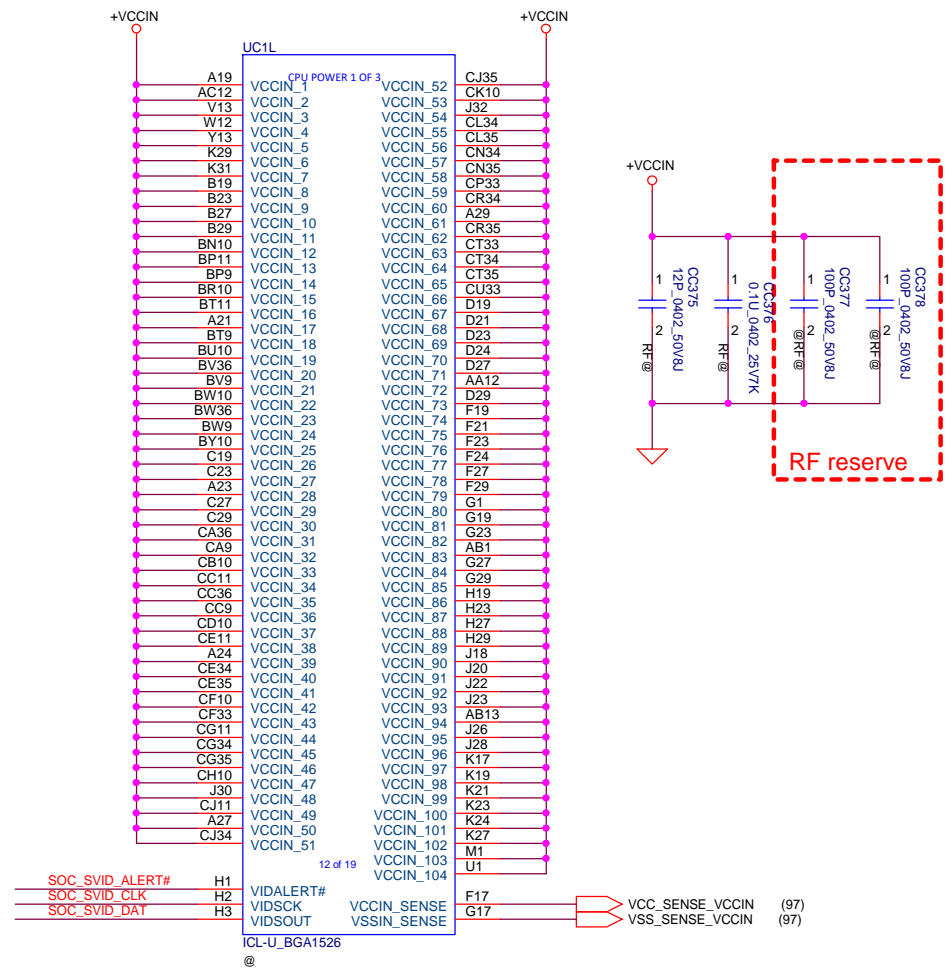


Figure above demonstrates Routing Illustration for SVID Topology, each trace from CPU to VR represents 3 signals: VIDSOUT, VIDSCK, VIDSALERT#.

Table 5-75. SVID Routing Guidelines

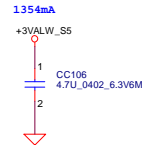
Segment	Tiline Type	Reference	Via Count	Max Length, mm	
				Segment	Total
M1	MS/SL/DSL	VSS		75	530
M2	MS/SL/DSL	VSS		380	
M3	MS/SL/DSL	VSS		75	
Topology Guidelines					
SVID Signals		VIDSOUT, VIDSCK, VIDSALERT#			
VIDSOUT platform resistors		Rpu1=100Ω, Rpu2=100Ω			
VIDSCK platform resistors		Rpu1=Empty, Rpu2=45Ω			
VIDSALERT# platform resistors		Rpu1=56Ω, Rpu2=Empty			
Platform resistors tolerances		± 5%			
Route ordering		When routing at minimum spacing route Alert between Data and Clock			



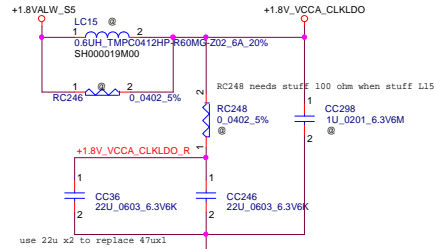
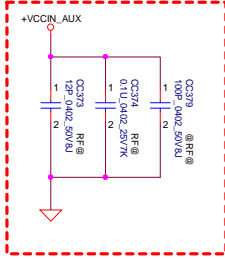
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2020/11/27		2020/11/27		Title	
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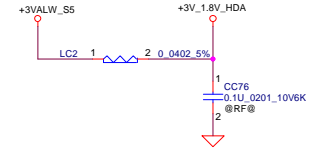
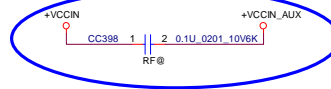
+3VALW



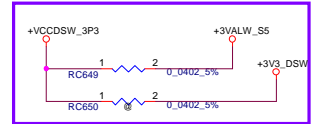
RF



For RF team cross note



20200624 Add power select for +VCCDSW_3P3



Ramps with VCCPrim 1.8V

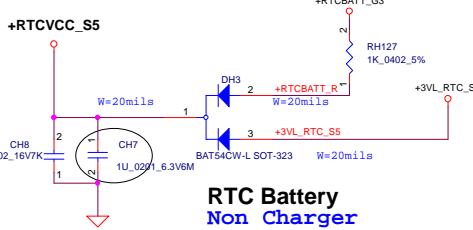
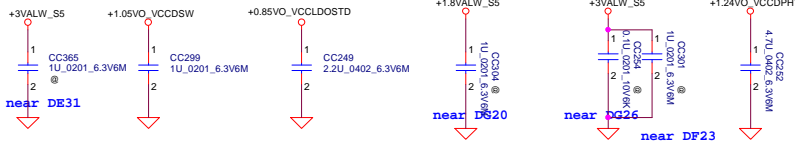
+RTCVCC_S5

+VCCDSW_3P3

+3V_1.8V_HDA

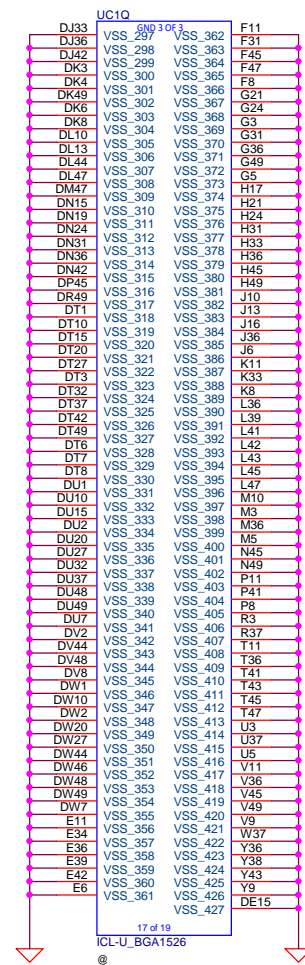
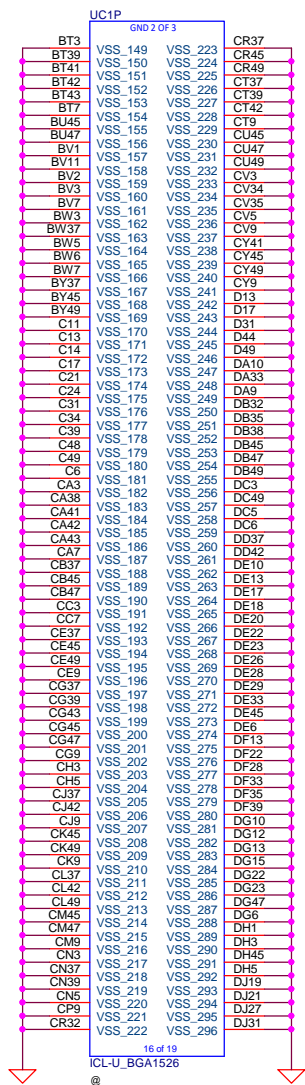
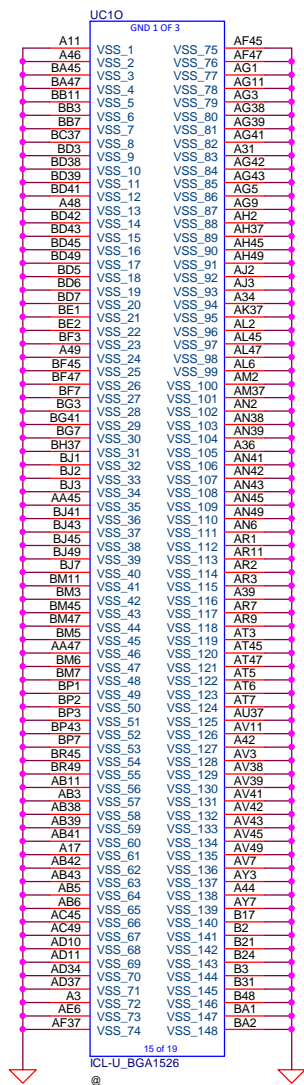
NOTE:
Need to follow SPI ROM Voltage

NOTE:
572631_ICL_PCH_LP_EDS_Vol_1_Rev_1p0
VCCPGPPR: Audio Power 3.3V, 1.8V, or 1.5V
Need to sync with codec VDDIO.
572907_ICL_UY_PDQ_Rev1p1
When configured as 3.3V or 1.8V, VCCPGPPR can be merged directly with either VCCPRIM_1P8 or VCCPRIM_3P3 depending on their operating voltage.



RTC Battery Non Charger

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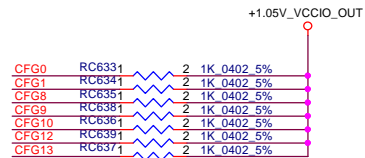


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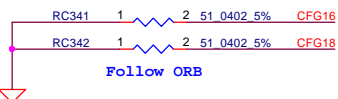
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Table 123. CFG Signals Functionality and Termination

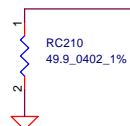
CFG	Description	Termination	Resistor
CFG0	CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted; — 1 = (Default) Normal Operation; No stall. — 0 = Stall.	Pull Up to VCCIO_OUT	1K Ohm
CFG1,8,9,10,12,13	RSVD	Pull Up to VCCIO_OUT	1K Ohm
CFG2,3,5,6,7,11,14,15	RSVD	No termination	N/A
CFG4	CFG[4]: eDP enable; — 1 = Disabled. — 0 = Enabled.	Pull Down	1K Ohm



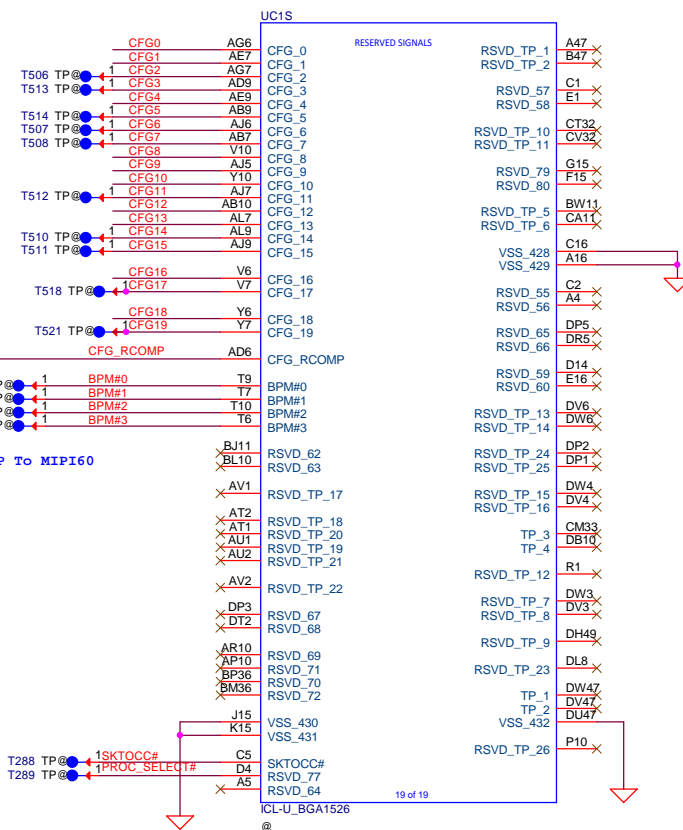
20200420 follow PDG modify CFG pull-high & reserve TP.



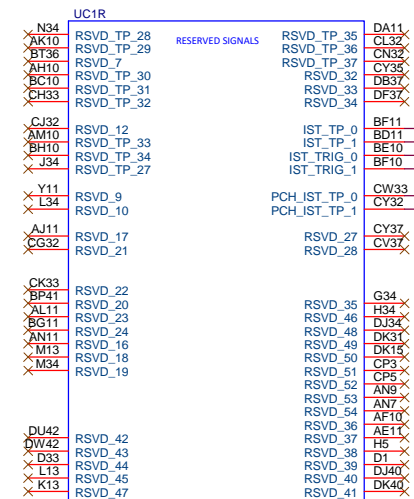
Follow ORB



RVP to MIP160

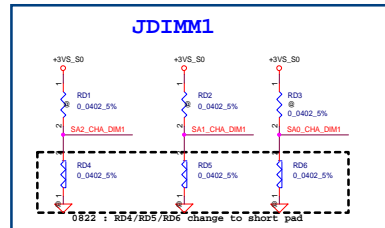


20200420 Add Test point for IST.



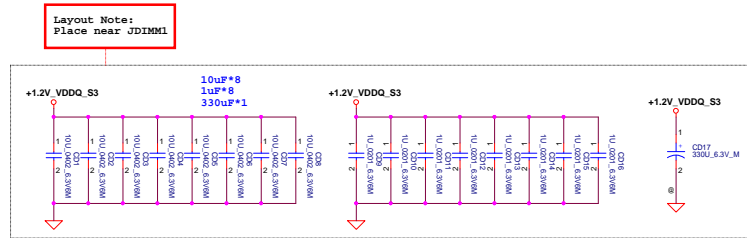
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Issued Date	2019/11/27	Deciphered Date	2020/11/27	ICL-U(13/13)RSVD,CFG	
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CHANNEL-A

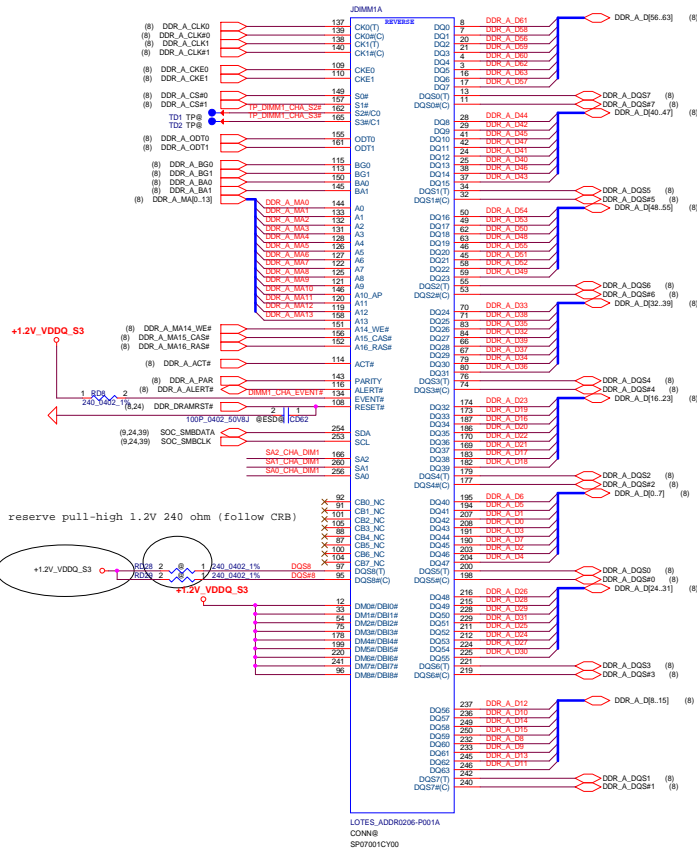


```
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS:0xA0
READ ADDRESS: 0xA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S
```

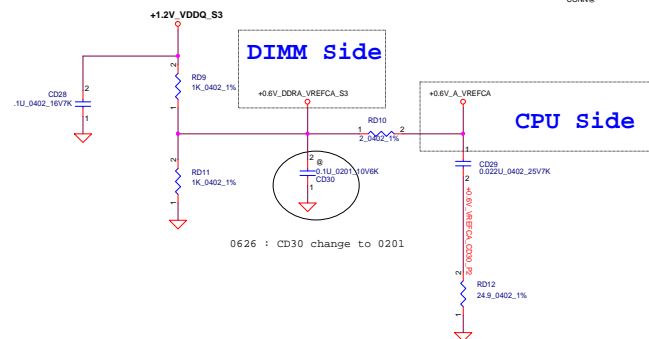
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM



(4.0 mm) REV TYPE



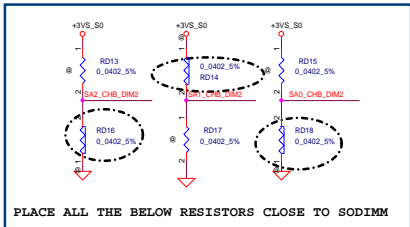
20200423 DDR DQ/DQS SWAP for Routing



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CHANNEL-B

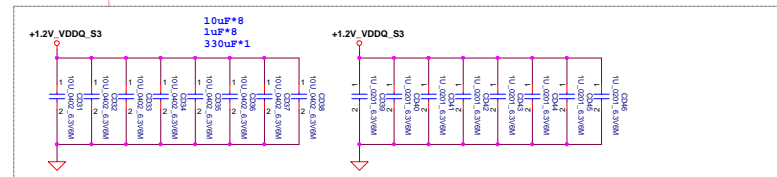
```
0801: correct RD14 Pin2
0822 : RD14/RD16/RD18 change to short pad
```



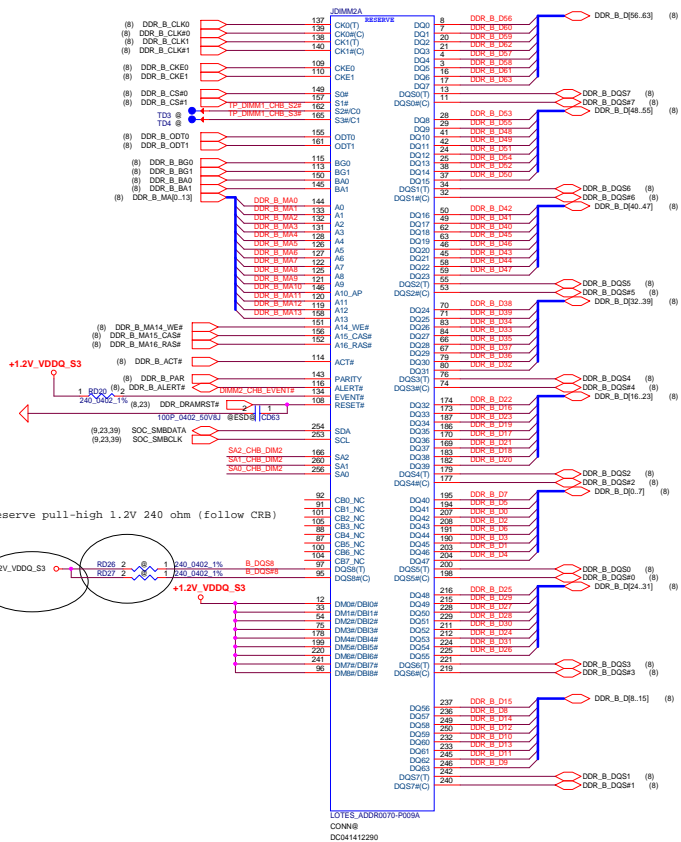
```
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS:0xA4
READ ADDRESS: 0xA5
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S
```

Layout Note:
Place near JDIMM2

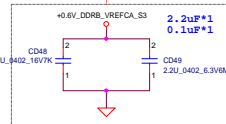
20200825 Correct BOM structure



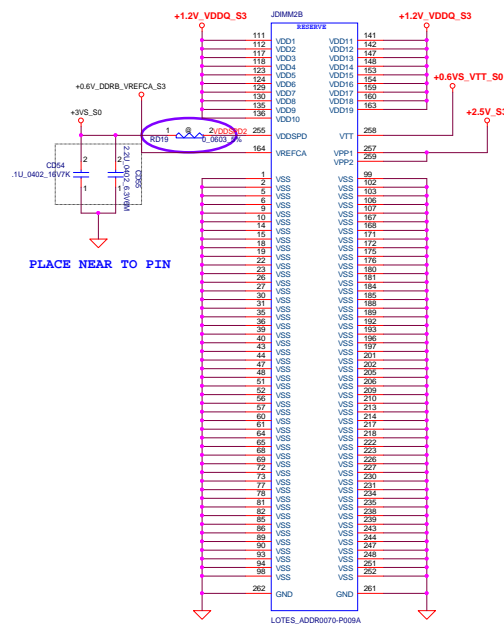
(8.0 mm)	REV	TYPE



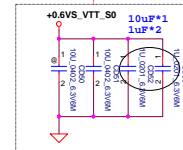
Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM2



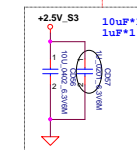
PLACE NEAR TO PIN



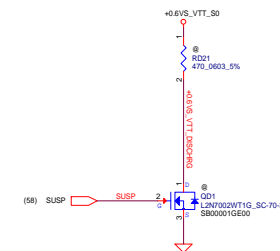
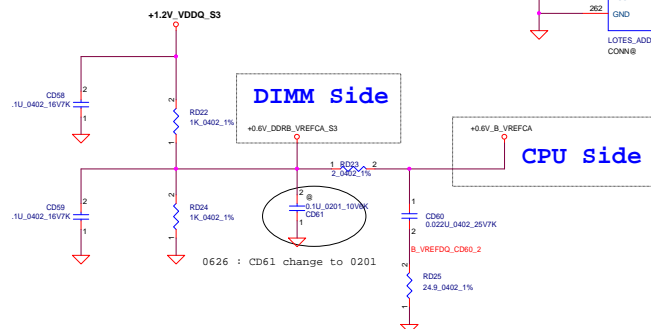
Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM2



20200423 DDR DQ/DQS SWAP for Routing



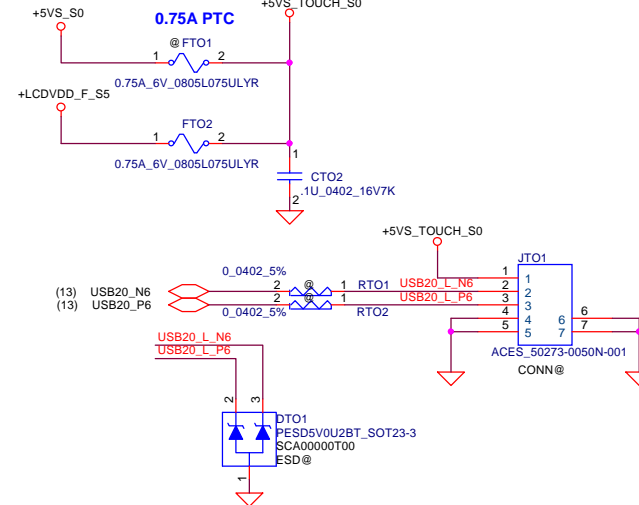
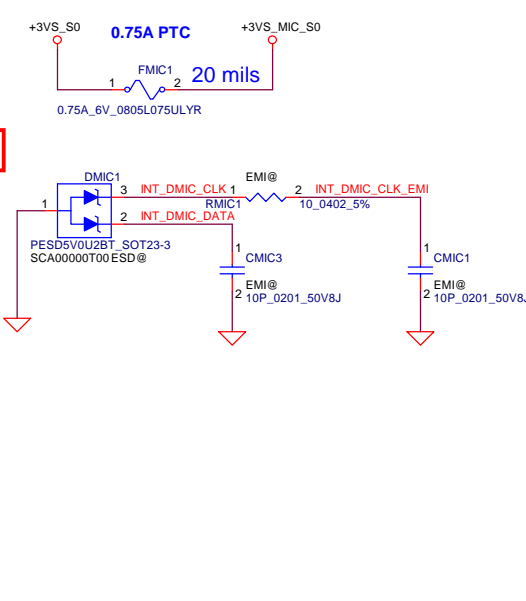
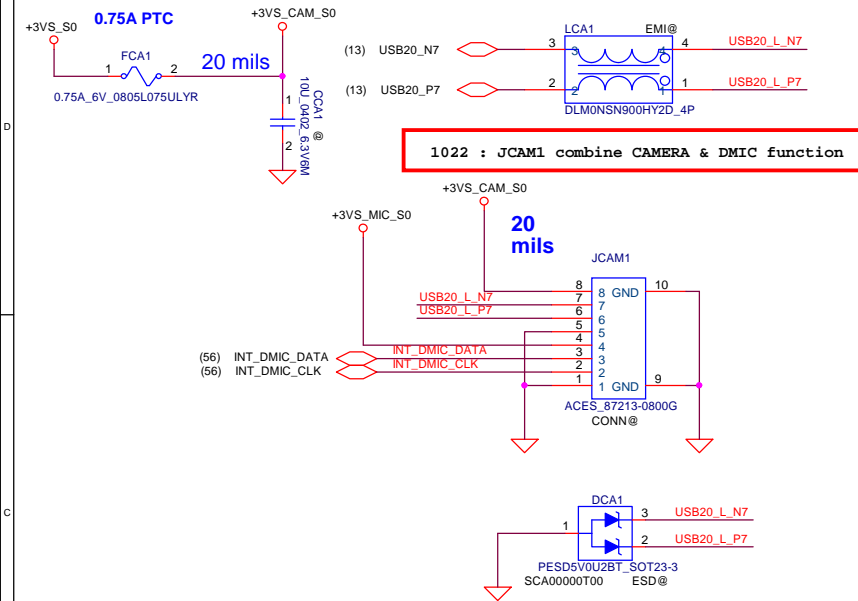
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Issued Date	2015/12/25	Deciphered Date	2015/12/31	DDR4 DIMMB
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			Custs	LA-K531P
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CAMERA

DMIC

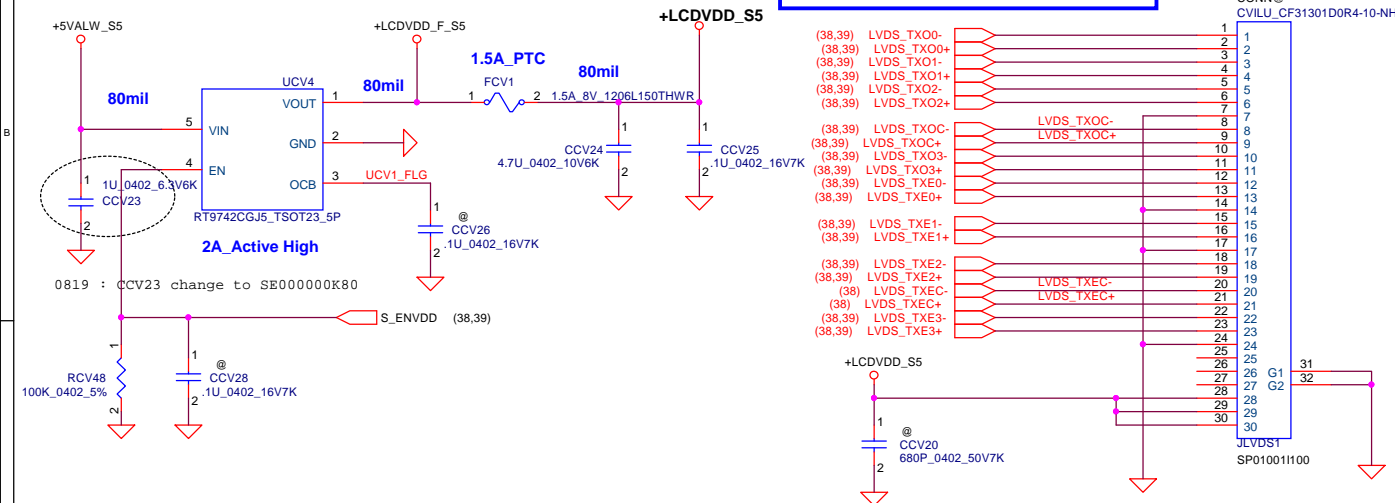
Touch



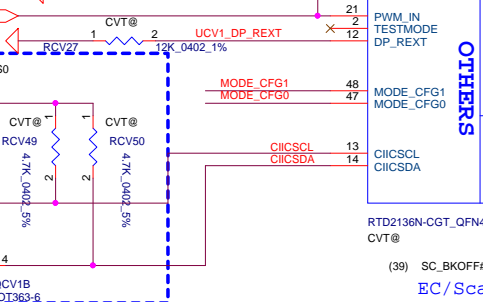
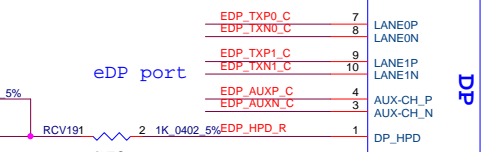
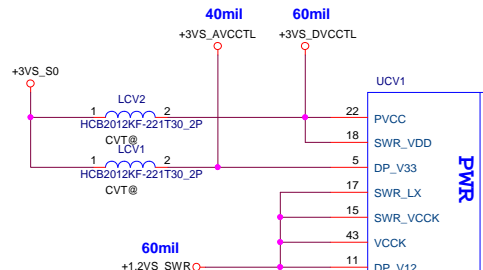
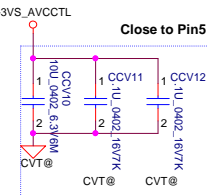
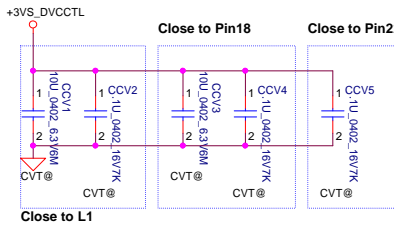
+LCDVDD Current Rating: Max=1500mA

RSC62/RSC63 near JLVD51 pin22 and 23

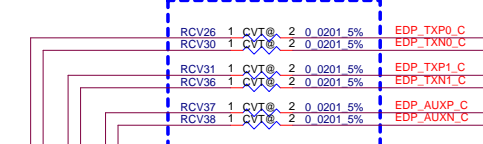
LVDS



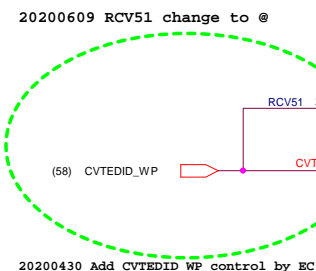
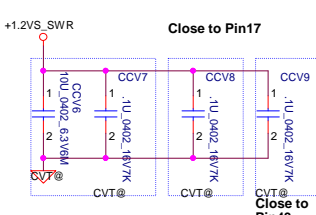
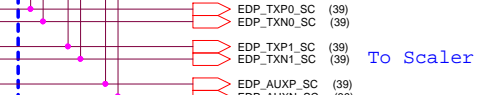
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/6/14	Deciphered Date	2019/6/14	Title	
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1031 : QCV1 / RCV49 / RCV50 change to POP (CVT SKU)



1115: RCV26,RCV30,RCV31,RCV36,RCV37,RCV38 change to 0201 type (DPB request)



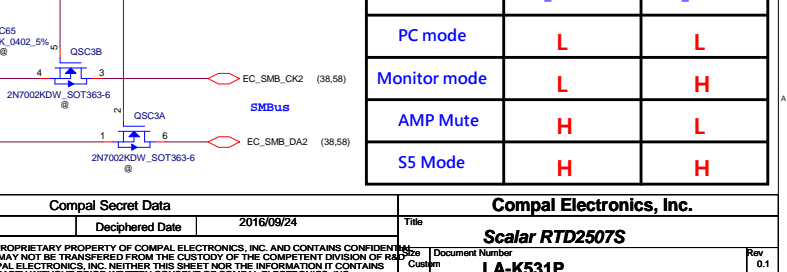
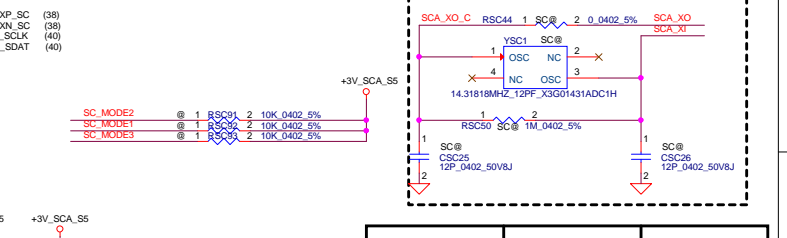
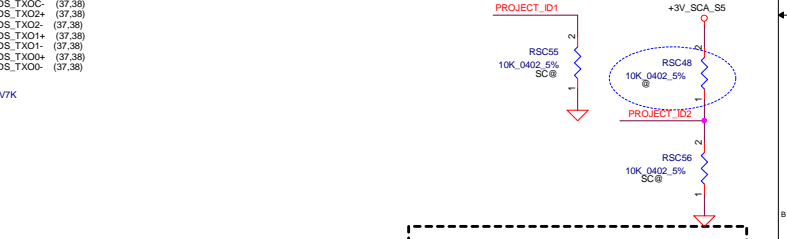
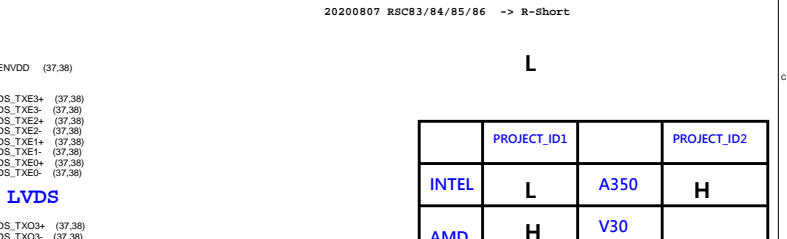
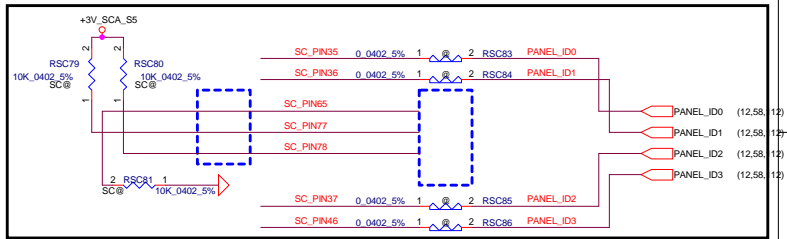
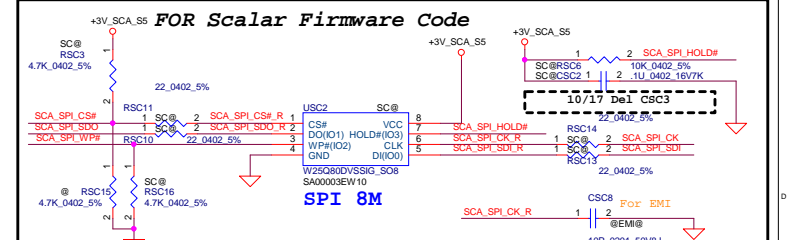
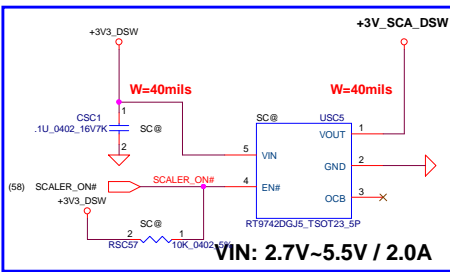
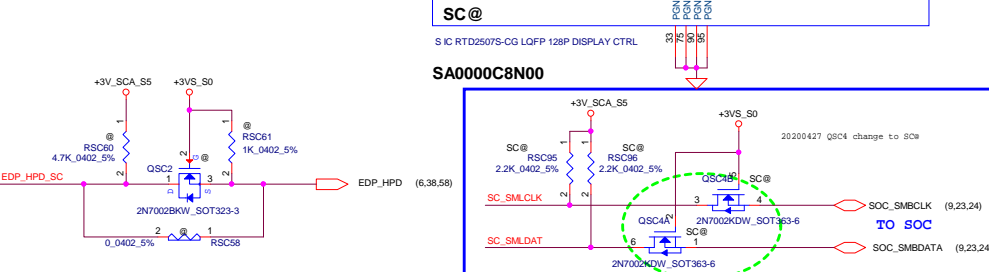
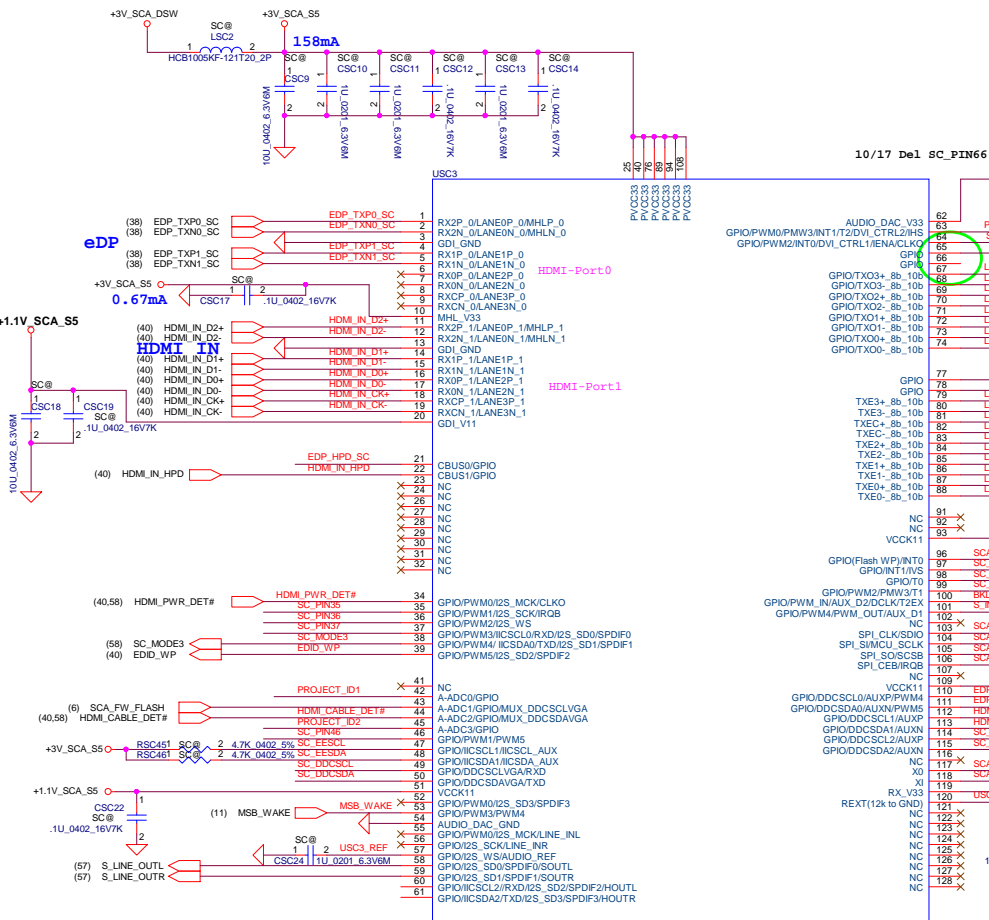
main source : LV9059GSP
second source : APL5933CKAI

480mA

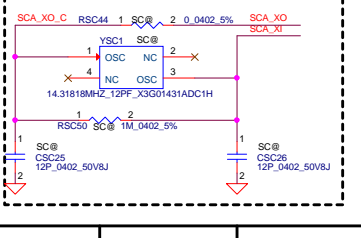
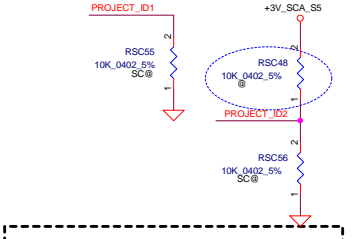
+3VALW TO +1.1VALW

Main Source : LV9059GSP
Vout = 0.8 * [1 + (14/35.7)] = 1.13V
IQ(typ) = 0.6mA, IQ(max) = 1.2mA
PD = (Vin - Vout) * Iout + Vin * IQ
= (3.3 - 1.13) * 0.48 + 3.3 * 0.0012 = 1.04556
θJA = 32.4 °C/W
PD * θJA = 1.04556 * 32.4 = 33.876 °C
(LNV SPEC <= 75 °C)

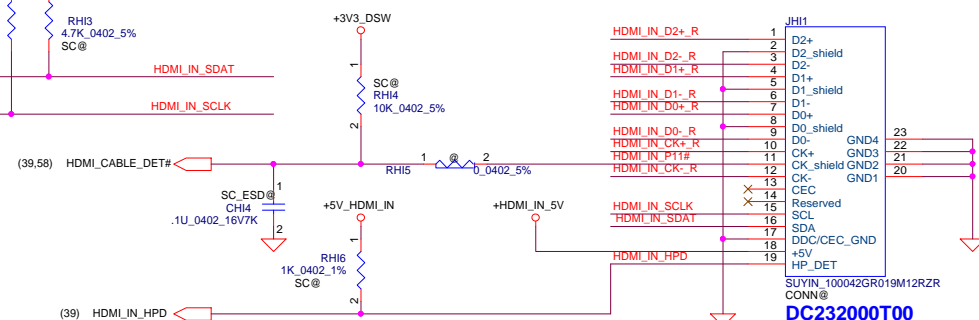
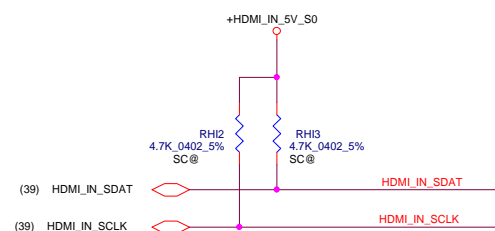
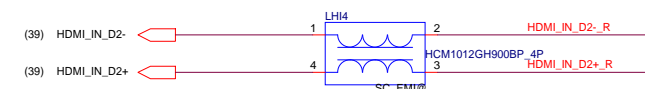
2nd Source : APL5933CKAI
Vout = 0.8 * [1 + (14/35.7)] = 1.13V
IQ(typ) = 20uA, IQ(max) = 30uA
PD = (Vin - Vout) * Iout + Vin * IQ
= (3.3 - 1.13) * 0.48 + 3.3 * 0.000000 = 1.04556 + 0.000099 = 1.045659
θJA = 50 °C/W
PD * θJA = 1.045659 * 50 = 52.28 °C
(LNV SPEC <= 75 °C)



	PROJECT_ID1	PROJECT_ID2
INTEL	L	A350
AMD	H	V30



	SC_MODE1	SC_MODE2
PC mode	L	L
Monitor mode	L	H
AMP Mute	H	L
S5 Mode	H	H

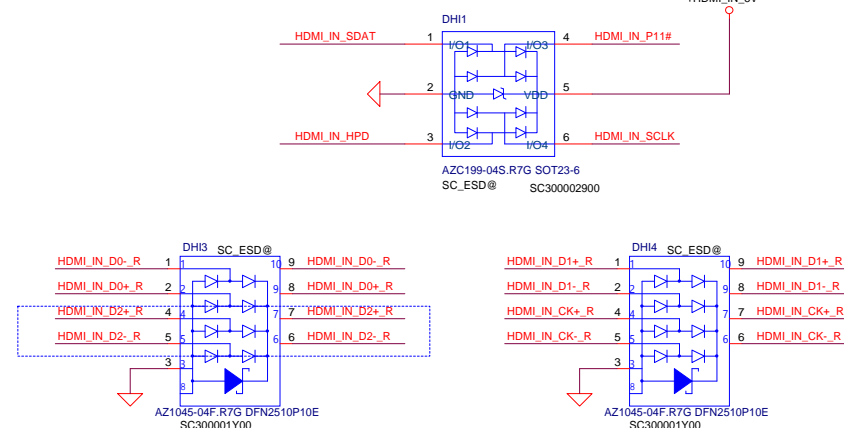


JH11		
1	D2+	
2	D2_shield	
3	D2+	
4	D1+	
5	D1_shield	
6	D1-	
7	D0-	
8	D0-	GND4 23
9	D0_shield	
10	CK+	GND3 21
11	CK_shield	GND2 20
12	CEC	
13	Reserved	
14	SCL	
15	SDA	
16	DDC/CEC_GND	
17	+5V	
18	HP_1004	
19		

SUVIN_1M0024GR019M12ZR

CONN@

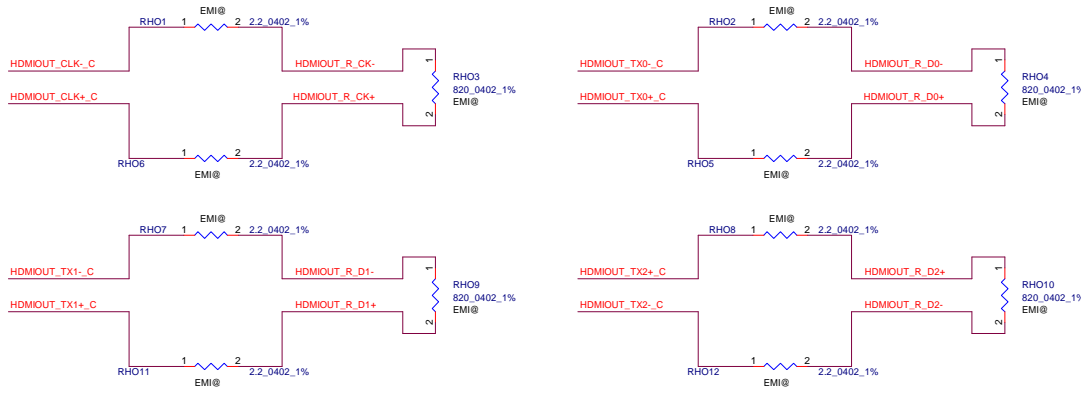
DC232000T00



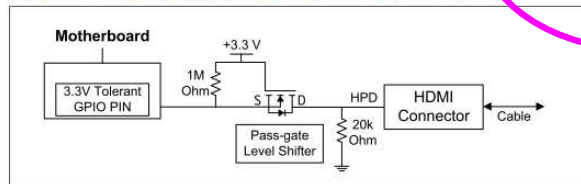
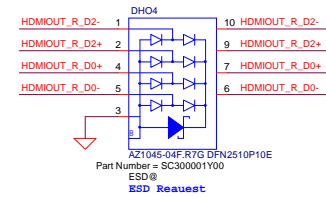
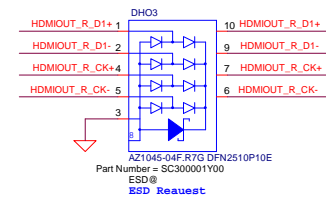
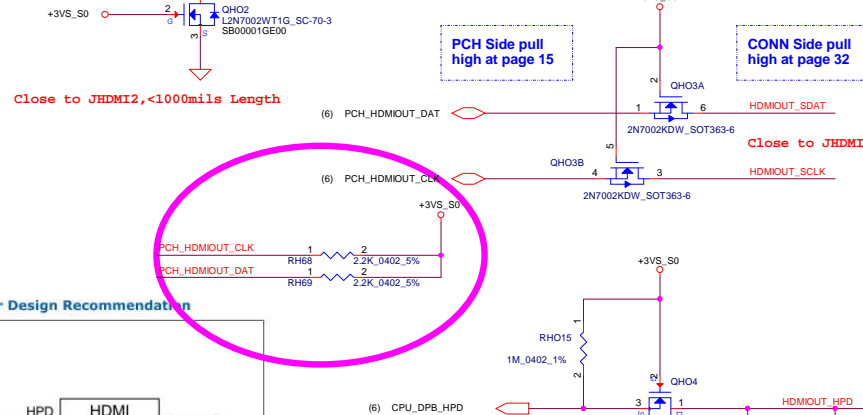
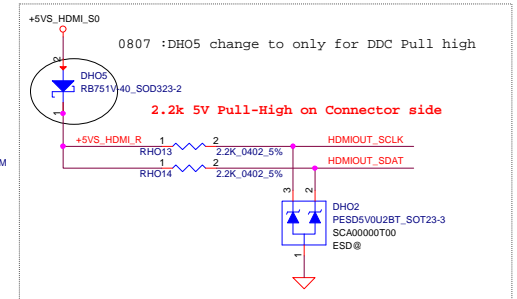
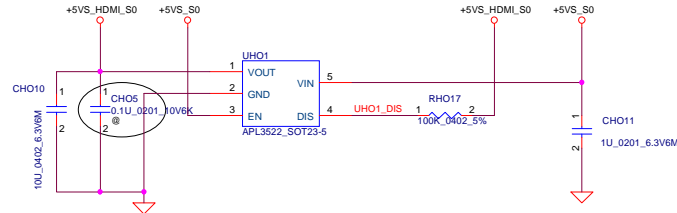
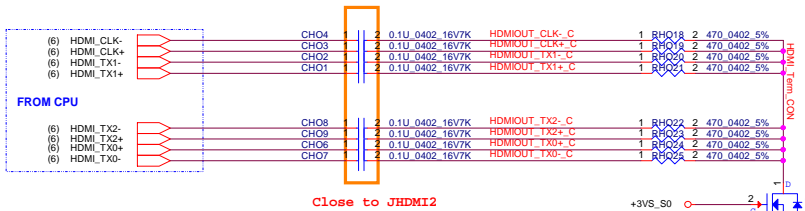
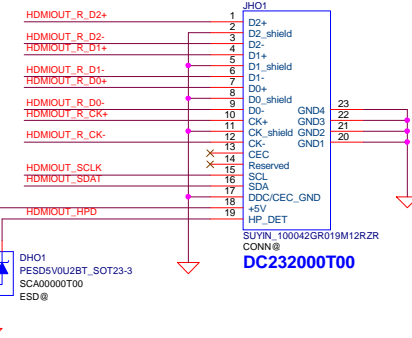
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				Size	Document Number	Rev
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1008: Remove co-layout choke LHO1,LHO2,LHO3,LHO4

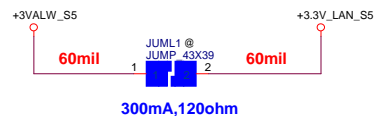


HDMI-OUT Connector



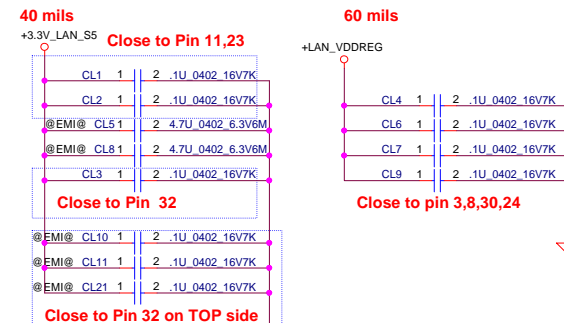
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				Size	Document Number	Rev
				LA-K531P		
				Date:	Tuesday, August 25, 2020	Sheet 41 of 121

WOL circuit (Connect +3V_LAN to +3VALW)



+3.3V_LAN rising time (10%~90%) need > 0.5ms and <100ms.

Power (Decoupling Cap.)

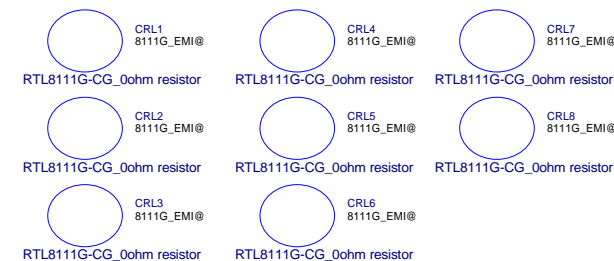


LED Status

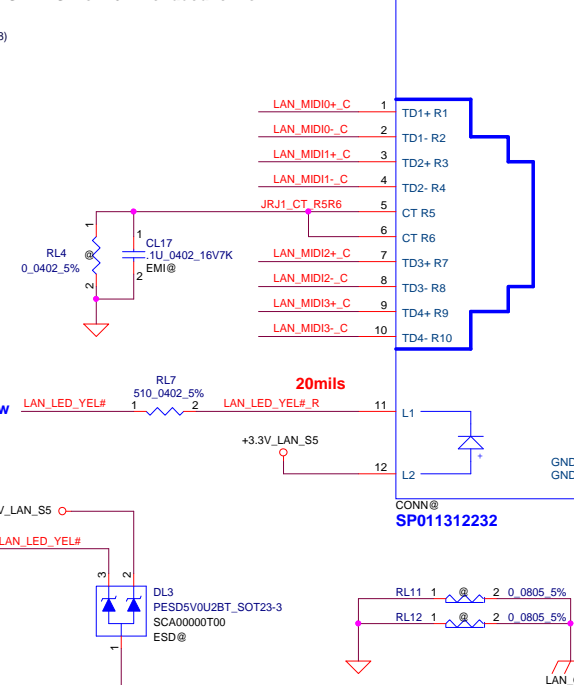
WOL	status	Yellow
don't care	No Link	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off
on	10M,inactive	
on	10M,active	
on	100M,inactive	
on	100M,active	
on	1G,inactive	
on	1G,active	

always on
blinking

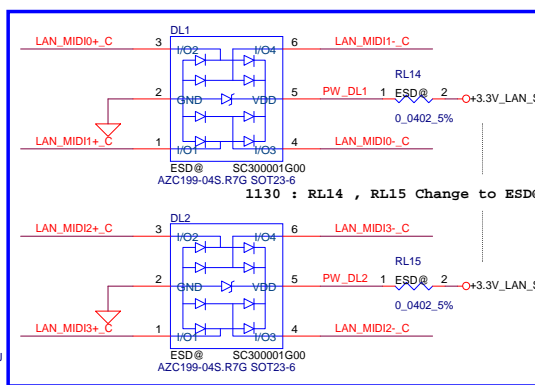
8111G resistor/8111H capacitor



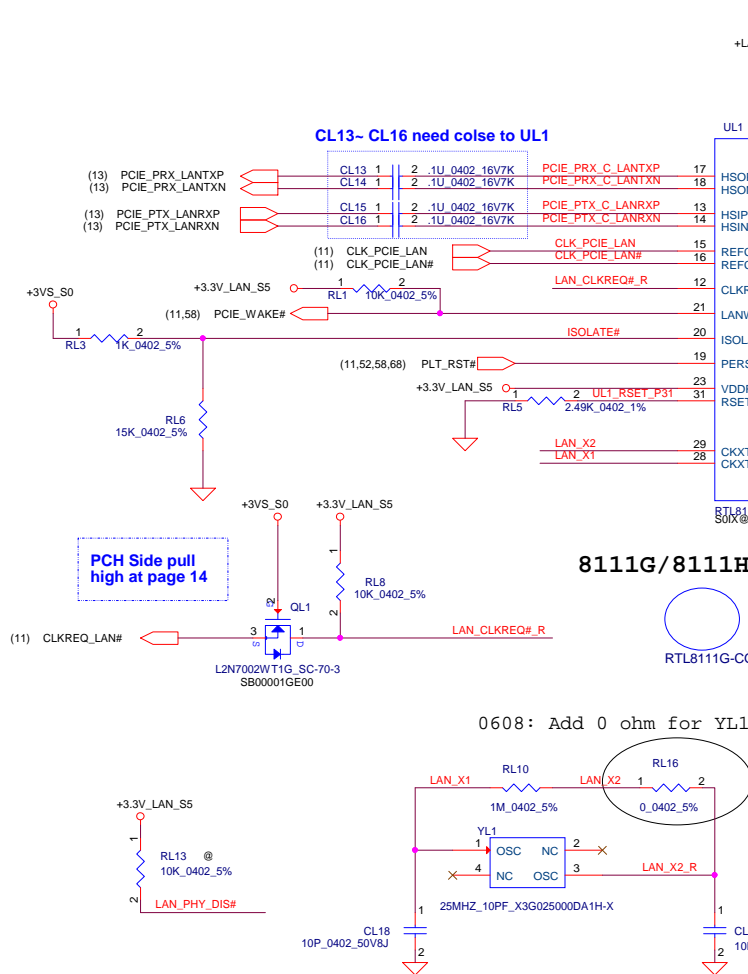
20200609 reassign CRL1~CRL8 BOM Structure for X4E

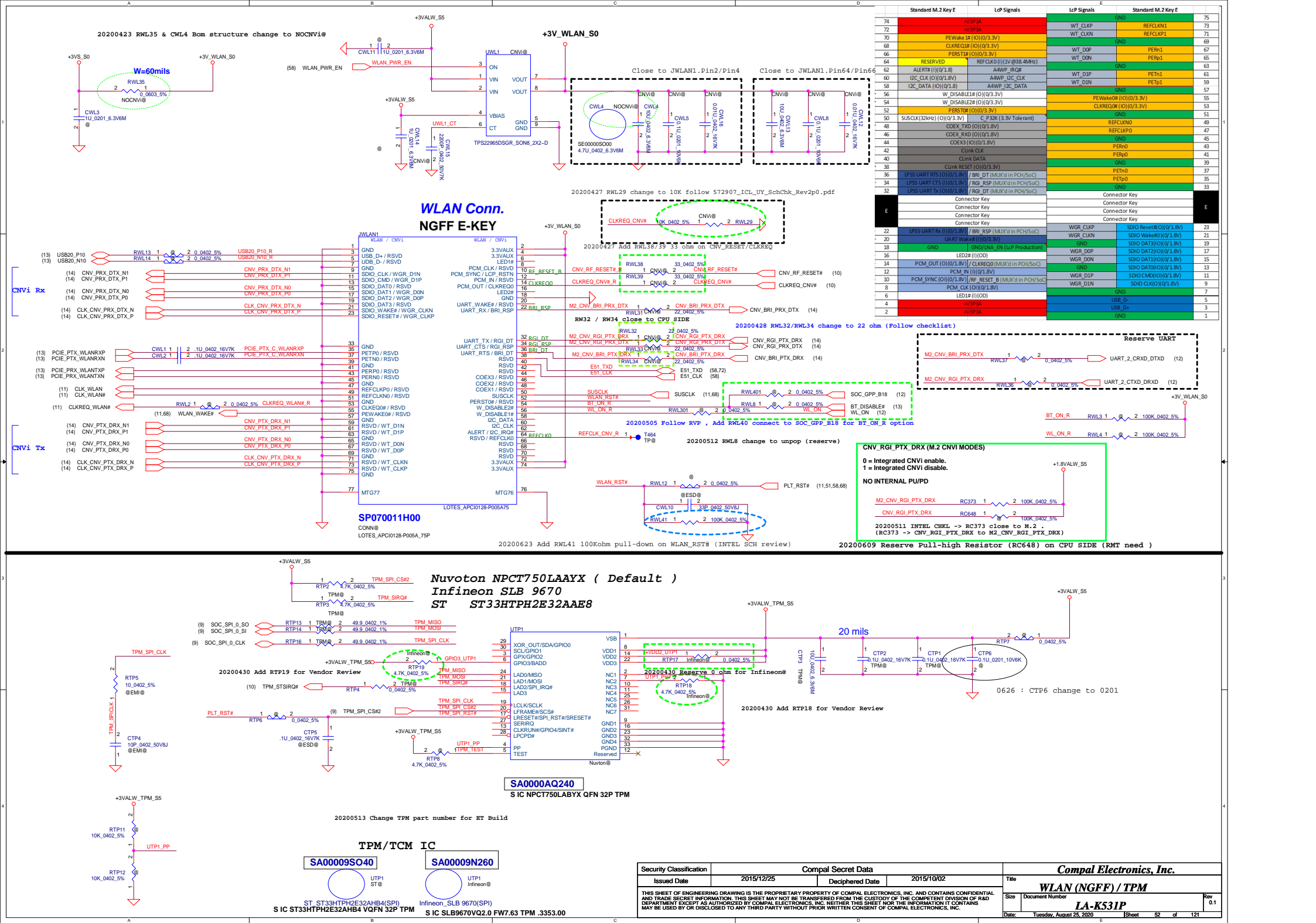


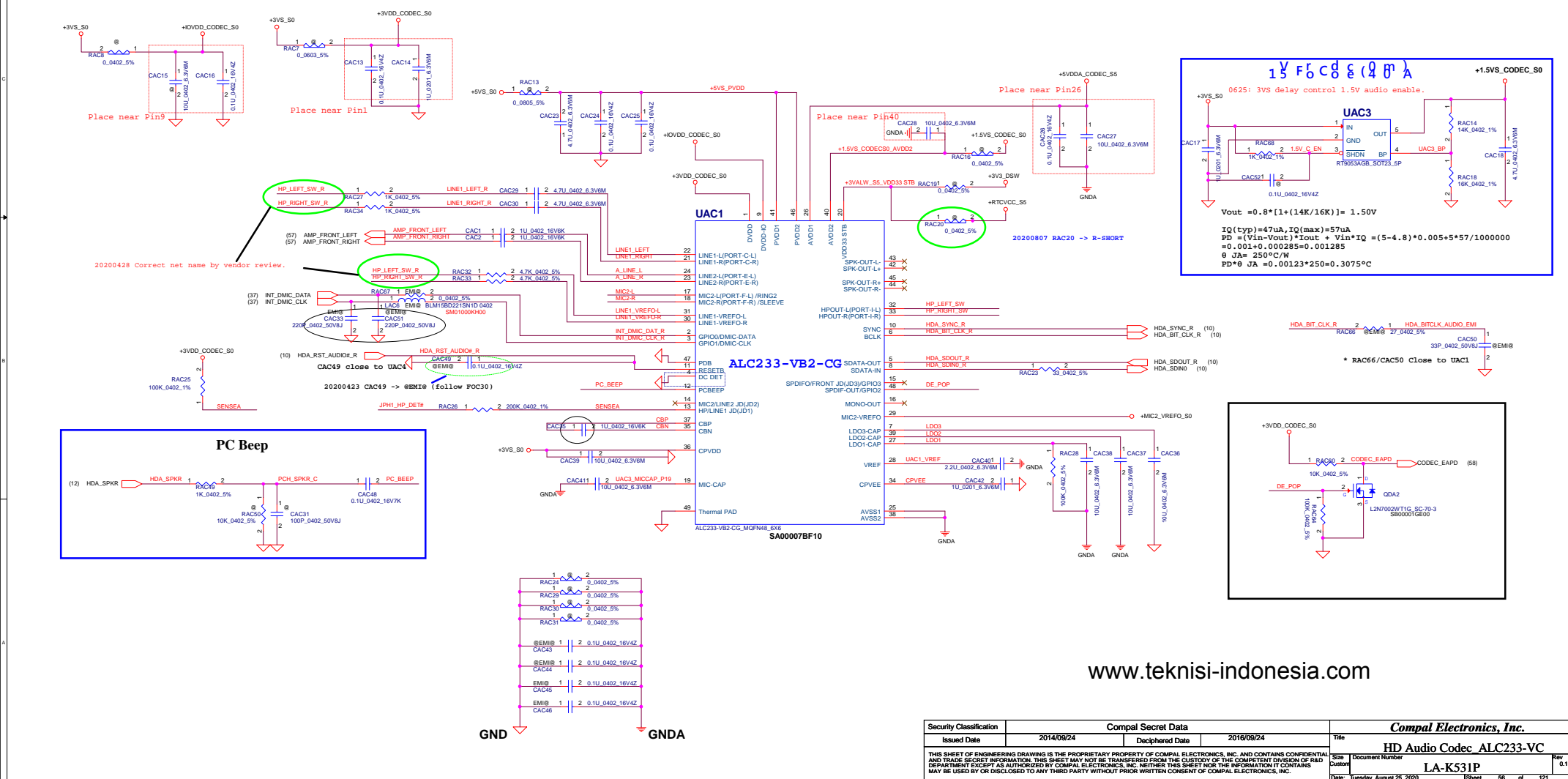
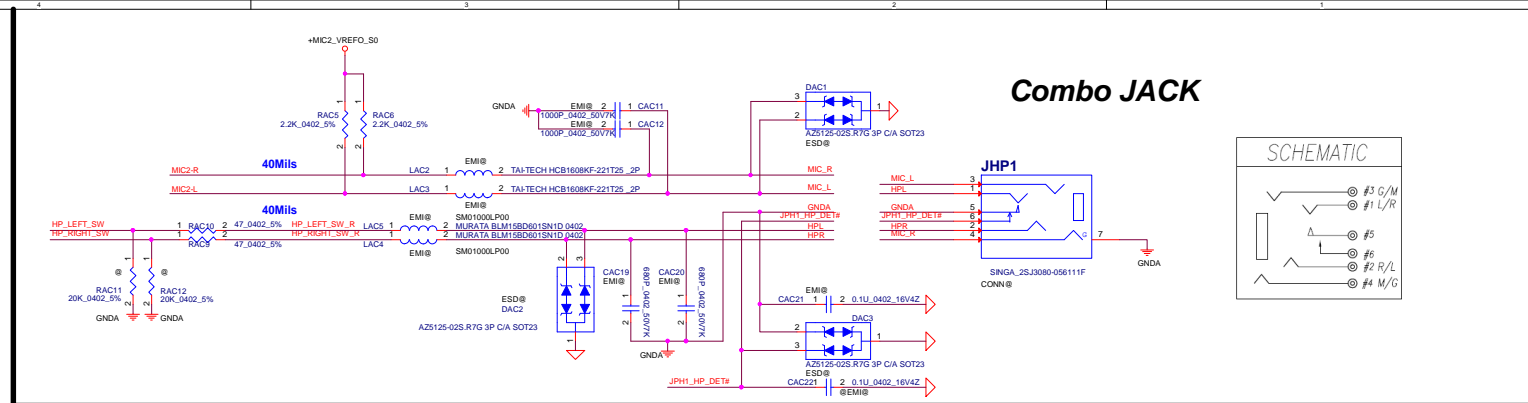
8111G/8111H LAN chip

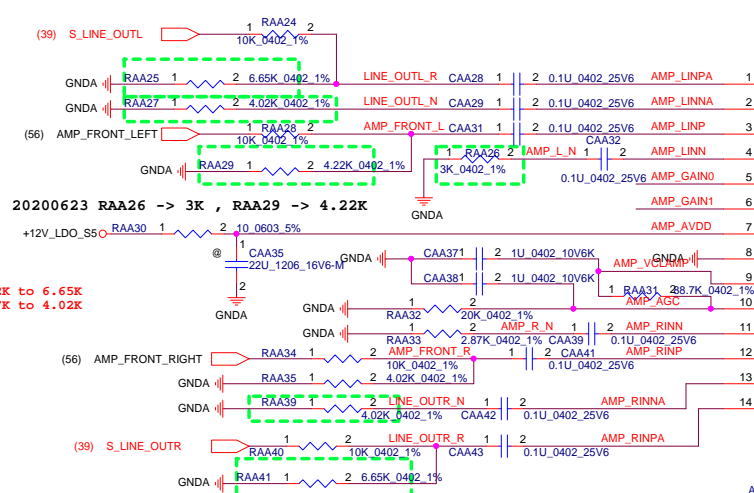
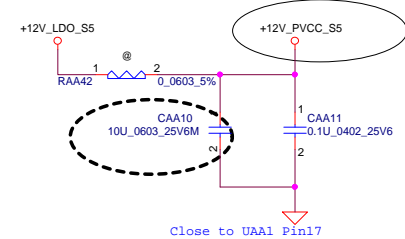
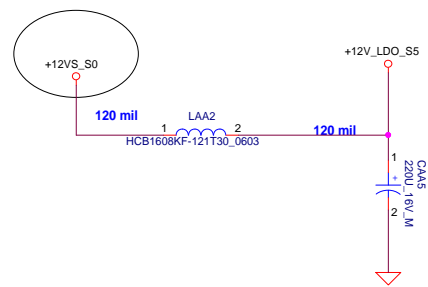


0608: Add 0 ohm for YL1





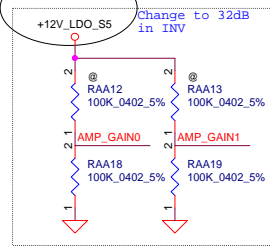




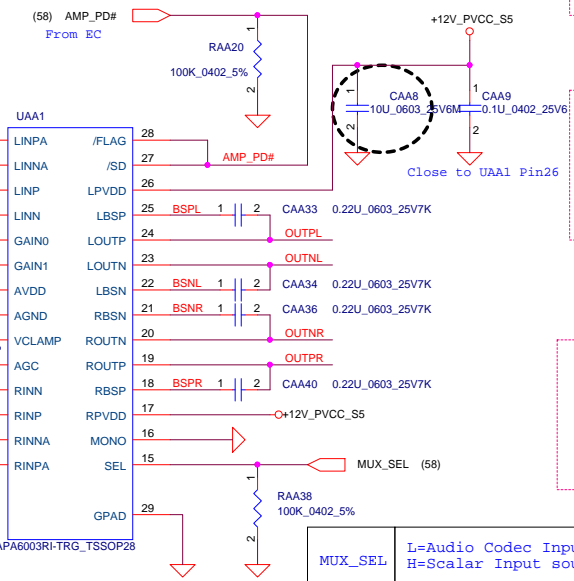
20200623 RAA26 -> 3K , RAA29 -> 4.22K

20200701 RAA25 / RAA41 -> 4.02K to 6.65K
RAA27 / RAA39 -> 2.87K to 4.02K
RAA29 -> 4.22K
RAA26 -> 3K

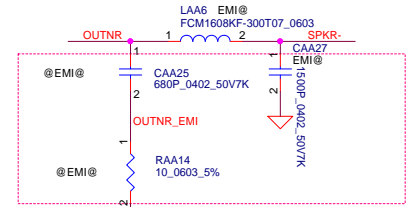
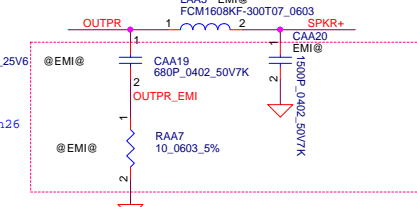
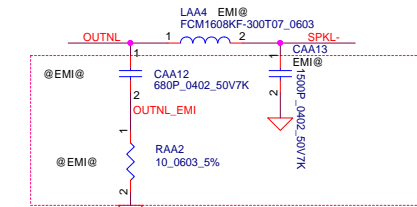
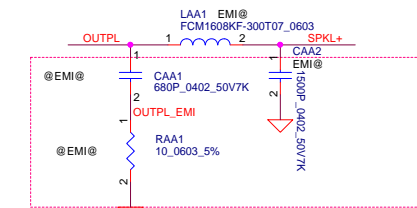
APA6003 for Speaker (CRB)



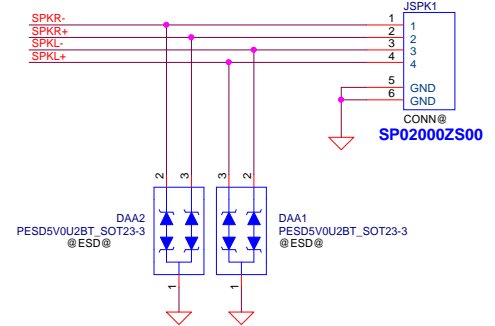
GAIN1	GAIN0	AV (inv)	INPUT IMPEDANCE
0	0	20dB	60Kohm
0	1	26dB	30Kohm
1	0	32dB	15Kohm
1	1	36dB	9Kohm

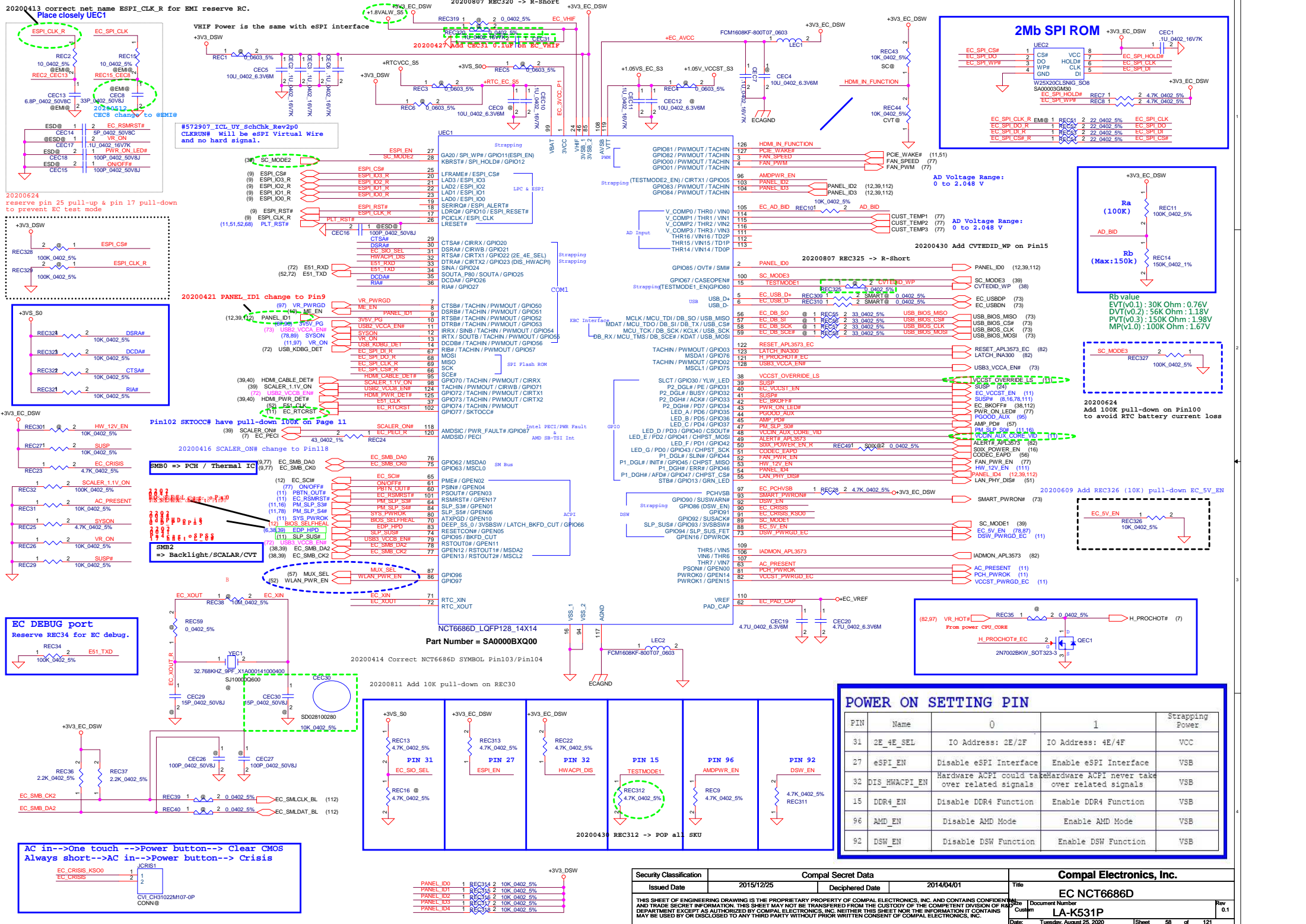


MUX_SEL L=Audio Codec Input source
H=Scalar Input source

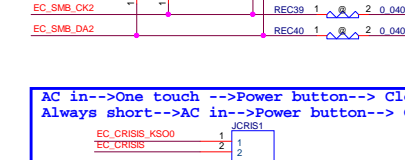
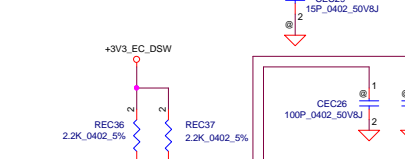
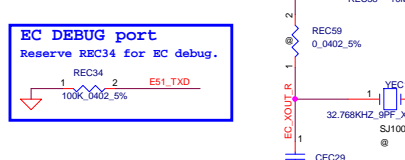
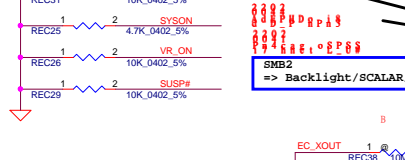
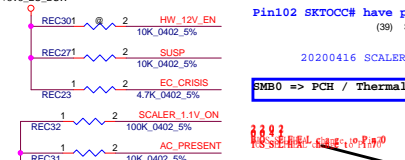
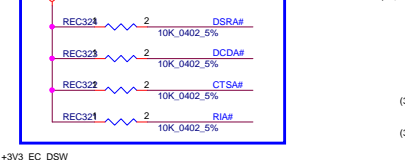
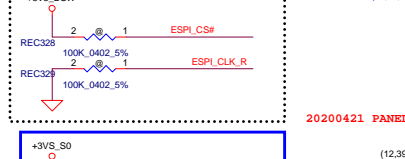
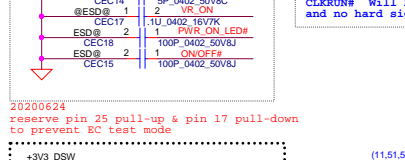
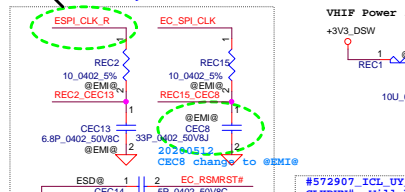


Speaker Conn.
3Wx2 4ohm Speaker

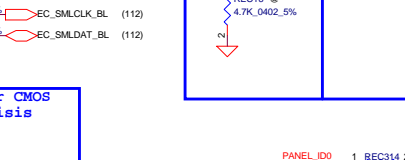
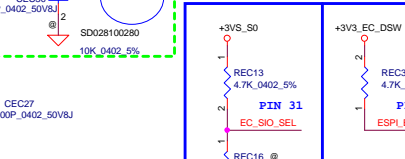
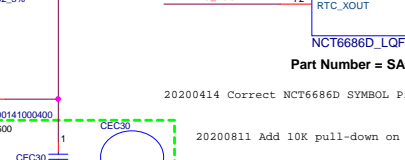
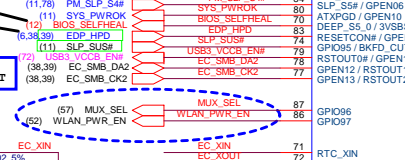
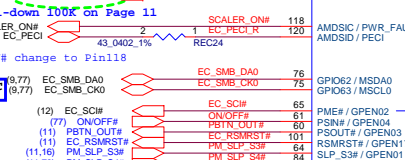
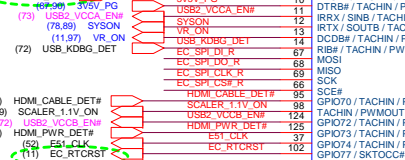
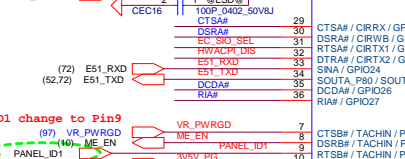
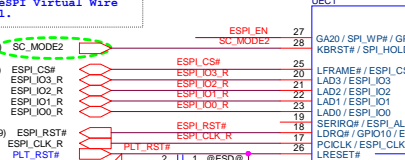
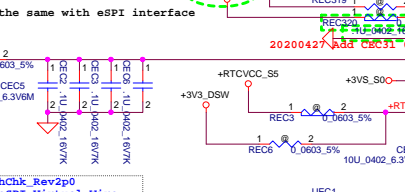




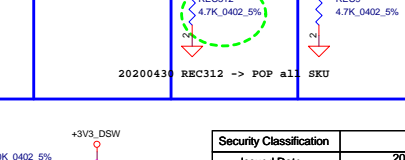
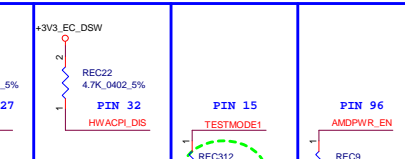
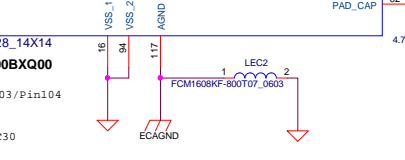
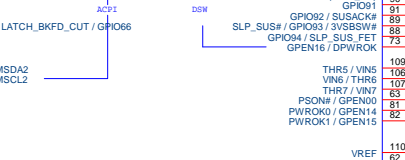
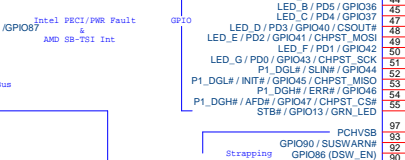
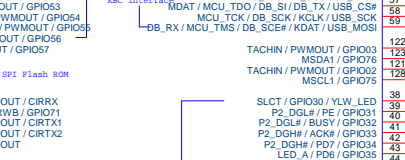
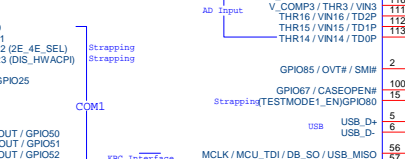
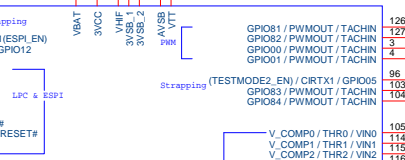
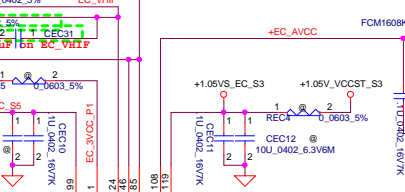
20200413 correct net name ESPI_CLK_R for EMI reserve RC.
Place closely UEC1



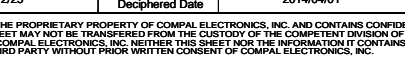
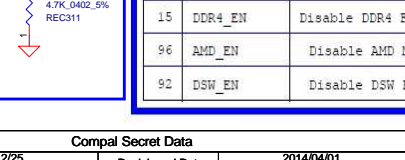
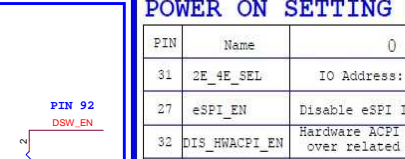
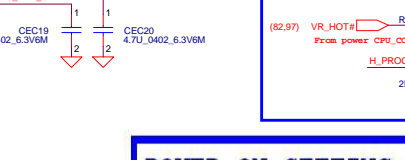
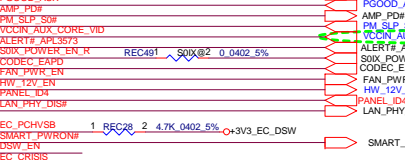
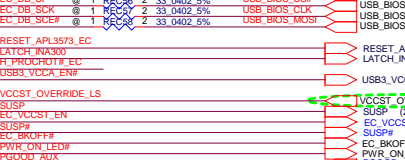
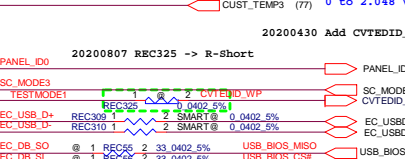
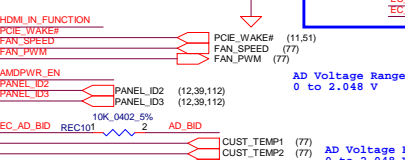
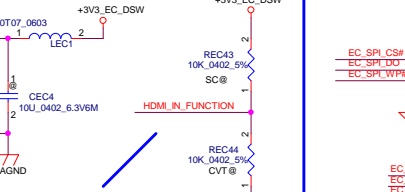
20200807 REC320 -> R-Short



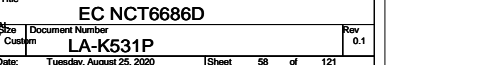
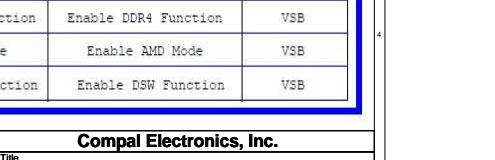
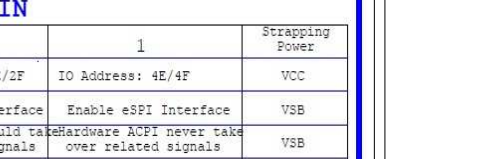
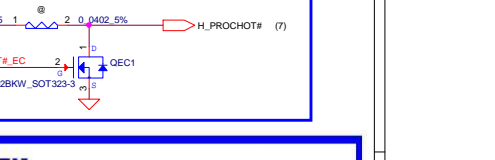
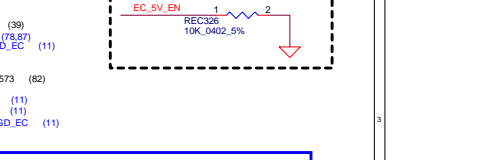
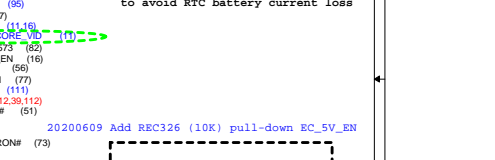
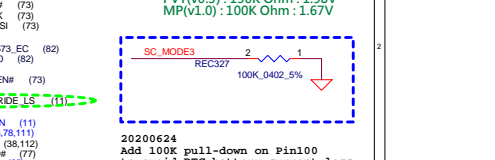
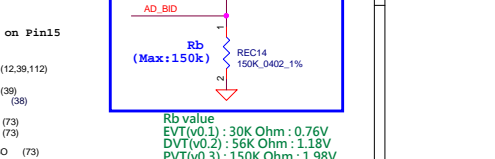
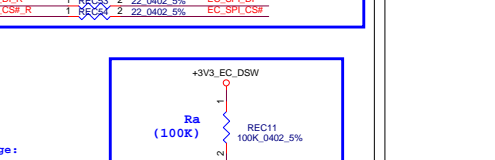
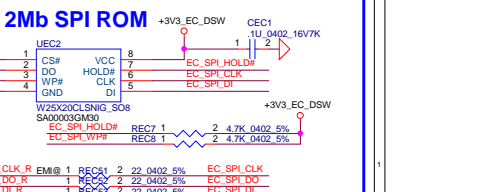
20200427 Add REC31 0.10K for EC_VHIF



20200430 Add CVT2ED_WP on Pin15



20200430 Add CVT2ED_WP on Pin15



POWER ON SETTING PIN

PIN	Name	0	1	Strapping Power
31	2E_4E_SEL	IO Address: 2E/2F	IO Address: 4E/4F	VCC
27	eSPI_EN	Disable eSPI Interface	Enable eSPI Interface	VSB
32	DIS_HWACPI_EN	Hardware ACPI could take over related signals	Hardware ACPI never take over related signals	VSB
15	DDR4_EN	Disable DDR4 Function	Enable DDR4 Function	VSB
96	AMD_EN	Disable AMD Mode	Enable AMD Mode	VSB
92	DSW_EN	Disable DSW Function	Enable DSW Function	VSB

366439_CNL_PCH_U_EDS_Vol_1_Rev_1.1				ECC02_061(WHL)	
Group	Sail	GPIU Number	GPIU Name	Signal name	External PU/PD
GPIU	BV36	GPIU0	BATLOW#	PM_BATLOW#	PU 8.2K to +3VALW_5S
	BV35	GPIU1	ACPRESENT#	AC_PRESENT#_B	PU 10K to +3VALW_5S (B)
	BV32	GPIU2	LAN_WAKE#	LAN_WAKE#	NC
	BV28	GPIU3	PAWRTW#	PAWRTW#	TP
	BV36	GPIU4	SIP_55#	PM_SIP_55#	PU 10K to +3VALW_5S
	BV27	GPIU5	SIP_54#	PM_SIP_54#	PU 10K to +3VALW_5S
	BV37	GPIU6	SIP_A#	NC	NC
	BV35	GPIU7	GPIU_7	SOC_GPIU7	PU 100K to +3VALW_5S
	BV32	GPIU8	SUSCLK	SUSCLK	NC
	BV30	GPIU9	PM_SIP_55#	PM_SIP_55#	TP
GPIU	BV29	GPIU10	SIP_55#	PM_SIP_55#	TP
	BV34	GPIU11	LAN_PHYC	NC	NC
	BV28	GPIU_A0	ECIM	ECIM	PU 10K to +3VALW_5S
	CA29	GPIU_A1	TIME_SYNC1	LPC_A00	LPC_A00
	BV29	GPIU_A2	LAD1	LPC_A01	LPC_A01
	BV27	GPIU_A3	LAD2	LPC_A02	LPC_A02
	BV27	GPIU_A4	LAD3	LPC_A03	LPC_A03
	CA28	GPIU_A5	LPC_FRAME#	LPC_FRAME#	LPC_FRAME#
	BV28	GPIU_A6	SERIRQ	SERIRQ	PU 8.2K to +3VALW_5S
	CC32	GPIU_A7	FIRQA#	SOC_GPIU_A7	PU 10K to +3VALW_5S
GPIU	BV30	GPIU_A8	CURRUP#	PM_CURRUP#	PU 8.2K to +3VALW_5S
	BV32	GPIU_A9	CLKOUT_LPC0	LPC_CLK0	LPC_CLK0
	BV30	GPIU_A10	FIRQA#	PM_CURRUP#	PU 8.2K to +3VALW_5S
	CA32	GPIU_A11	PM_CURRUP#	PM_CURRUP#	PU 8.2K to +3VALW_5S
	BV37	GPIU_A12	PM_CURRUP#	PM_CURRUP#	PU 8.2K to +3VALW_5S
	BV34	GPIU_A13	SUSWARM#	SUSWARM#	PU 10K to +3VALW_5S (B)
	CA27	GPIU_A14	SUSWARM#	SUSWARM#	PU 10K to +3VALW_5S (B)
	BV32	GPIU_A15	SUSACK#	SUSACK#	NC
	BV31	GPIU_A16	SD_IP#_SEL	NC	NC
	BV36	GPIU_A17	SD_VDD1_PWR_EN#	NC	NC
GPIU	BV35	GPIU_A18	ISH_GPD	NC	NC
	BV34	GPIU_A19	ISH_GP1	NC	NC
	CA37	GPIU_A20	ISH_GP2	NC	NC
	CA36	GPIU_A21	ISH_GP3	NC	NC
	CA35	GPIU_A22	ISH_GP4	NC	NC
	CA34	GPIU_A23	ISH_GP5	NC	NC
	CB36	GPIU_B0	NC	NC	NC
	CB35	GPIU_B1	NC	NC	NC
	CC36	GPIU_B2	VREALERT#	SOC_VREALERT#	PU 10K to +3VALW_5S (B)
	CB34	GPIU_B3	CVU_DP1	NC	NC
GPIU	CC35	GPIU_B4	CVU_DP3	NC	NC
	CF32	GPIU_B5	SRCLKREQ0#	CLKREQ_V0AM	PU 10K to +3VALW_5S
	CE32	GPIU_B6	SRCLKREQ01#	CLKREQ_LAN#	PU 10K to +3VALW_5S
	CF30	GPIU_B7	SRCLKREQ03#	CLKREQ_WLAN#	PU 10K to +3VALW_5S
	CE31	GPIU_B8	SRCLKREQ03#	NC	NC
	CE30	GPIU_B9	SRCLKREQ04#	CLKREQ_S0H	PU 10K to +3VALW_5S
	CF31	GPIU_B10	SRCLKREQ03#	NC	NC
	CC37	GPIU_B11	EXT_PWR_GATE#	NC	NC
	BV37	GPIU_B12	SIP_55#	PM_SIP_55#	TP
	BV35	GPIU_B13	PLTRST#	SOC_PLTRST#	PU 10K to +3VALW_5S
GPIU	CF35	GPIU_B14	SPKR	HDA_SPKR	PU 2.2K to +3VALW_5S (B)
	CC27	GPIU_B15	GSPIU_CSD#	NC	NC
	CE28	GPIU_B16	GSPIU_CLK	GPIU_B16	TP
	CC27	GPIU_B17	GSPIU_MISO	NC	NC
	CE29	GPIU_B18	GSPIU_MOSI	GSPIU_MOSI	TP
	CA31	GPIU_B19	GSPIU_CSD#	NC	NC
	CC29	GPIU_B20	GSPIU_CLK	NC	NC
	CC30	GPIU_B21	GSPIU_MISO	NC	NC
	CA30	GPIU_B22	GSPIU_MOSI	GSPIU_MOSI	TP
	CC34	GPIU_B23	SMLALERT#	SOC_SMLALERT#	PU 100K to +3VALW_5S
GPIU	CK14	GPIU_C0	SMBCLK	PM_SMBCLK	PU 2.2K to +3VALW_5S
	CK15	GPIU_C1	SMBDATA	PM_SMBDATA	PU 2.2K to +3VALW_5S
	CK16	GPIU_C2	SMBALERT#	SOC_SMBALERT#	PU 10K to +3VALW_5S
	CK17	GPIU_C3	SMBCLK	SOC_SMBCLK	PU 1K to +3VALW_5S
	CK18	GPIU_C4	SMBDATA	SOC_SMBDATA	PU 1K to +3VALW_5S
	CK19	GPIU_C5	SMBALERT#	SOC_SMBALERT#	PU 1K to +3VALW_5S
	CK20	GPIU_C6	SMBCLK	SOC_SMBCLK	PU 1K to +3VALW_5S
	CK21	GPIU_C7	SMBDATA	SOC_SMBDATA	PU 1K to +3VALW_5S
	CK22	GPIU_C8	SMBALERT#	SOC_SMBALERT#	PU 1K to +3VALW_5S
	CK23	GPIU_C9	SMBCLK	SOC_SMBCLK	PU 1K to +3VALW_5S

366439_CNL_PCH_U_EDS_Vol_1_Rev_1.1				ECC02_061(WHL)	
Group	Sail	GPIU Number	GPIU Name	Signal name	External PU/PD
GPIU	BV36	GPIU0	BATLOW#	PM_BATLOW#	PU 8.2K to +3VALW_5S
	BV35	GPIU1	ACPRESENT#	AC_PRESENT#_B	PU 10K to +3VALW_5S (B)
	BV32	GPIU2	LAN_WAKE#	LAN_WAKE#	NC
	BV28	GPIU3	PAWRTW#	PAWRTW#	TP
	BV36	GPIU4	SIP_55#	PM_SIP_55#	PU 10K to +3VALW_5S
	BV27	GPIU5	SIP_54#	PM_SIP_54#	PU 10K to +3VALW_5S
	BV37	GPIU6	SIP_A#	NC	NC
	BV35	GPIU7	GPIU_7	SOC_GPIU7	PU 100K to +3VALW_5S
	BV32	GPIU8	SUSCLK	SUSCLK	NC
	BV30	GPIU9	PM_SIP_55#	PM_SIP_55#	TP
GPIU	BV29	GPIU10	SIP_55#	PM_SIP_55#	TP
	BV34	GPIU11	LAN_PHYC	NC	NC
	BV28	GPIU_A0	ECIM	ECIM	PU 10K to +3VALW_5S
	CA29	GPIU_A1	TIME_SYNC1	LPC_A00	LPC_A00
	BV29	GPIU_A2	LAD1	LPC_A01	LPC_A01
	BV27	GPIU_A3	LAD2	LPC_A02	LPC_A02
	BV27	GPIU_A4	LAD3	LPC_A03	LPC_A03
	CA28	GPIU_A5	LPC_FRAME#	LPC_FRAME#	LPC_FRAME#
	BV28	GPIU_A6	SERIRQ	SERIRQ	PU 8.2K to +3VALW_5S
	CC32	GPIU_A7	FIRQA#	SOC_GPIU_A7	PU 10K to +3VALW_5S
GPIU	BV30	GPIU_A8	CURRUP#	PM_CURRUP#	PU 8.2K to +3VALW_5S
	BV32	GPIU_A9	CLKOUT_LPC0	LPC_CLK0	LPC_CLK0
	BV30	GPIU_A10	FIRQA#	PM_CURRUP#	PU 8.2K to +3VALW_5S
	CA32	GPIU_A11	PM_CURRUP#	PM_CURRUP#	PU 8.2K to +3VALW_5S
	BV37	GPIU_A12	PM_CURRUP#	PM_CURRUP#	PU 8.2K to +3VALW_5S
	BV34	GPIU_A13	SUSWARM#	SUSWARM#	PU 10K to +3VALW_5S (B)
	CA27	GPIU_A14	SUSWARM#	SUSWARM#	PU 10K to +3VALW_5S (B)
	BV32	GPIU_A15	SUSACK#	SUSACK#	NC
	BV31	GPIU_A16	SD_IP#_SEL	NC	NC
	BV36	GPIU_A17	SD_VDD1_PWR_EN#	NC	NC
GPIU	BV35	GPIU_A18	ISH_GPD	NC	NC
	BV34	GPIU_A19	ISH_GP1	NC	NC
	CA37	GPIU_A20	ISH_GP2	NC	NC
	CA36	GPIU_A21	ISH_GP3	NC	NC
	CA35	GPIU_A22	ISH_GP4	NC	NC
	CA34	GPIU_A23	ISH_GP5	NC	NC
	CB36	GPIU_B0	NC	NC	NC
	CB35	GPIU_B1	NC	NC	NC
	CC36	GPIU_B2	VREALERT#	SOC_VREALERT#	PU 10K to +3VALW_5S (B)
	CB34	GPIU_B3	CVU_DP1	NC	NC
GPIU	CC35	GPIU_B4	CVU_DP3	NC	NC
	CF32	GPIU_B5	SRCLKREQ0#	CLKREQ_V0AM	PU 10K to +3VALW_5S
	CE32	GPIU_B6	SRCLKREQ01#	CLKREQ_LAN#	PU 10K to +3VALW_5S
	CF30	GPIU_B7	SRCLKREQ03#	CLKREQ_WLAN#	PU 10K to +3VALW_5S
	CE31	GPIU_B8	SRCLKREQ03#	NC	NC
	CE30	GPIU_B9	SRCLKREQ04#	CLKREQ_S0H	PU 10K to +3VALW_5S
	CF31	GPIU_B10	SRCLKREQ03#	NC	NC
	CC37	GPIU_B11	EXT_PWR_GATE#	NC	NC
	BV37	GPIU_B12	SIP_55#	PM_SIP_55#	TP
	BV35	GPIU_B13	PLTRST#	SOC_PLTRST#	PU 10K to +3VALW_5S
GPIU	CF35	GPIU_B14	SPKR	HDA_SPKR	PU 2.2K to +3VALW_5S (B)
	CC27	GPIU_B15	GSPIU_CSD#	NC	NC
	CE28	GPIU_B16	GSPIU_CLK	GPIU_B16	TP
	CC27	GPIU_B17	GSPIU_MISO	NC	NC
	CE29	GPIU_B18	GSPIU_MOSI	GSPIU_MOSI	TP
	CA31	GPIU_B19	GSPIU_CSD#	NC	NC
	CC29	GPIU_B20	GSPIU_CLK	NC	NC
	CC30	GPIU_B21	GSPIU_MISO	NC	NC
	CA30	GPIU_B22	GSPIU_MOSI	GSPIU_MOSI	TP
	CC34	GPIU_B23	SMLALERT#	SOC_SMLALERT#	PU 100K to +3VALW_5S
GPIU	CK14	GPIU_C0	SMBCLK	PM_SMBCLK	PU 2.2K to +3VALW_5S
	CK15	GPIU_C1	SMBDATA	PM_SMBDATA	PU 2.2K to +3VALW_5S
	CK16	GPIU_C2	SMBALERT#	SOC_SMBALERT#	PU 10K to +3VALW_5S
	CK17	GPIU_C3	SMBCLK	SOC_SMBCLK	PU 1K to +3VALW_5S
	CK18	GPIU_C4	SMBDATA	SOC_SMBDATA	PU 1K to +3VALW_5S
	CK19	GPIU_C5	SMBALERT#	SOC_SMBALERT#	PU 1K to +3VALW_5S
	CK20	GPIU_C6	SMBCLK	SOC_SMBCLK	PU 1K to +3VALW_5S
	CK21	GPIU_C7	SMBDATA	SOC_SMBDATA	PU 1K to +3VALW_5S
	CK22	GPIU_C8	SMBALERT#	SOC_SMBALERT#	PU 1K to +3VALW_5S
	CK23	GPIU_C9	SMBCLK	SOC_SMBCLK	PU 1K to +3VALW_5S

System

PLT_RST#

EC

EC

ESPI_CLK

PLT_RST#/TPM_SPI_RST

TPM

SOC_SPI_0_CLK/TPM_SPI

GPP_H1	CM30	GPP_H3	I242_RXD CMV_BT_I25_SDO	NC	
	CF27	GPP_H4	I2C2_SDA	NC	
	CF29	GPP_H5	I2C2_SCL	NC	
	CM27	GPP_H6	I243_SDA	NC	
	CM28	GPP_H7	I2C3_SCL	NC	
	CM30	GPP_H8	I2C4_SDA	NC	
	CM31	GPP_H9	I2C4_SCL	NC	
	CM27	GPP_H10	I2C3_SDA ISA_I2C3_SDA	NC	
	CM29	GPP_H11	I2C5_SCL ISM_I2C3_SCL	GPP_H11	TP
	CM28	GPP_H12	M2_SKT2_CFG0	NC	
	CF28	GPP_H13	M2_SKT2_CFG1	NC	
	CM28	GPP_H14	M2_SKT2_CFG2	NC	
	CM28	GPP_H15	M2_SKT2_CFG3	NC	
	CM26	GPP_H16		NC	
	CF26	GPP_H17		NC	
	CM27	GPP_H18	CPU_C10_GATE#	SOC_C10_GATE#	PU 10K to +3VALW_5S (B)
	CM27	GPP_H19	WAKE#_CPU	NC	
	CM25	GPP_H20	WPSCLKOUT_1	NC	
	CF25	GPP_H21		SOC_GPP_H21	PU 4.7K to +3VALW_5S
	CM26	GPP_H22		NC	
CM26	GPP_H23		NC		

SM

Intel PCH (WHL-U)

PM_SMBCLK

PM_SMBDATA

Host SMBus

EC_SMB_CK0

EC_SMB_DA0

EC Nuvoton NCT6685

EC_SMB_CK2

EC_SMB_DA2

Host SMBus

LCD

EC_SMLCLK

Security Classification
Issued Date
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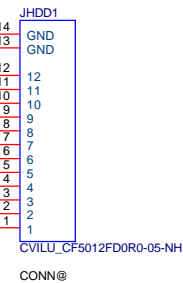
20200505 SATA Redriver Caps change power source to +UHDD3_VDD

20200417 Add RHDD17 between SATA Redriver VDD to +3VS_S0.

SATA HDD Conn. (FFC)

0704: JHDD1 Pin8 Pin7 Swap

SATA_RPTX_C_P0
SATA_RPTX_C_N0
SATA_RPRX_C_P0
SATA_RPRX_C_N0



CONN@

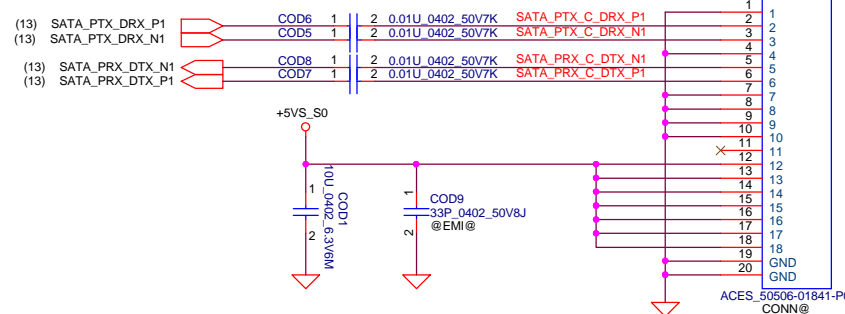
1008: For DFB request change footprint to cvilu_cf5012fd0r0-05-nh 12p-s

0626 : CHD2 change to 0201

teknisi-indonesia.com

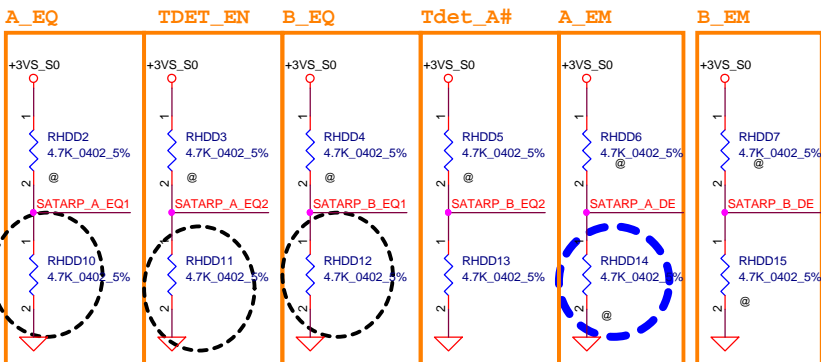
SATA ODD Conn. (FFC)

Place CAP close to JODD1 <100mil



ACES_50506-01841-P01
CONN@

0626 : HDD Redriver change to PI3EQX6741STZDEX
0628 : FAE suggest default adjustment setting Pin let it floating.

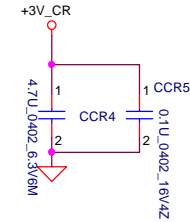
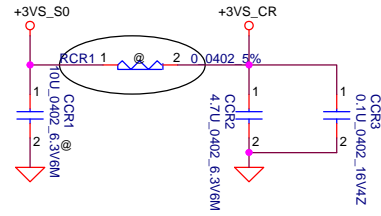
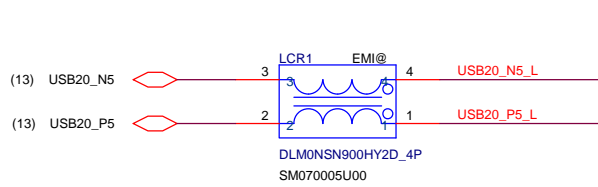


20200703 RHDD14 change to @

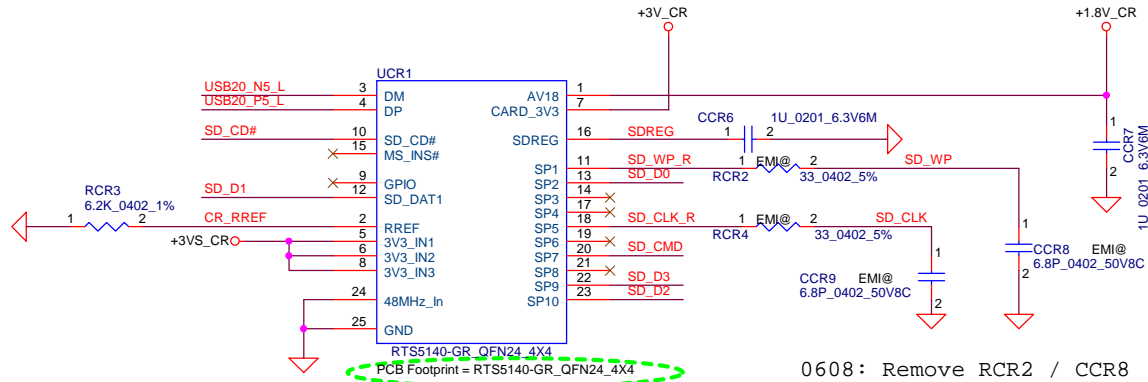
0817 : reference FAE test result
The setting was changed like below:
Pin9: A_EM=low, RHDD14=4.7kohm
Pin17: A_EQ=Low, RHDD10=4.7kohm
Pin18: TDET_EN=low, RHDD11=4.7kohm
Pin19: B_EQ=Low, RHDD12=4.7kohm

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/25	Deciphered Date	2013/09/01	Title	HDD+redriver/ODD
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				Date:	Tuesday, August 25, 2020
				Sheet	67 of 121

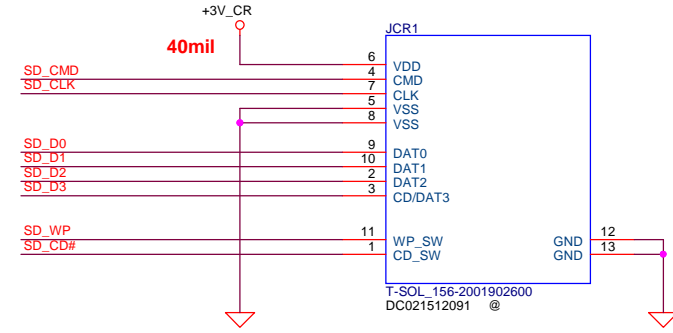
0822 : RCR1 change to short pad



CCR4,CCR5 place close to JCR1.6

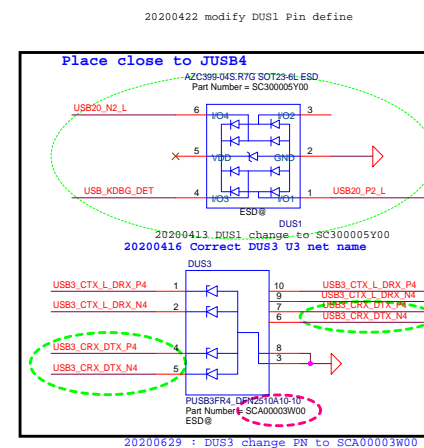
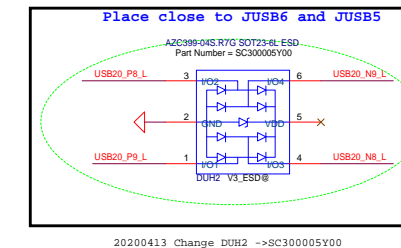
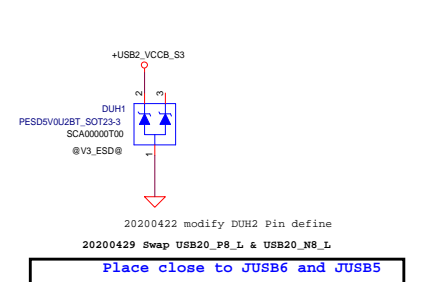


0608: Remove RCR2 / CCR8

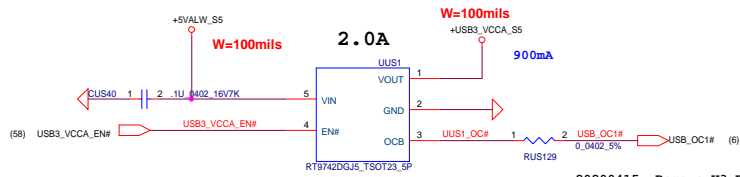


20200428 UCR1 change footprint to RTS5140-GR-QFN24_4X4

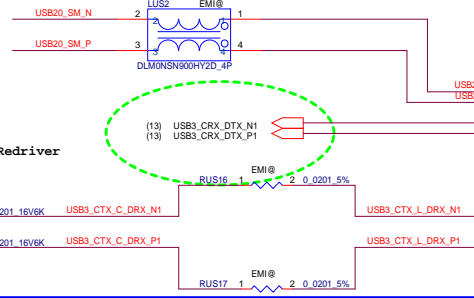
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Issued Date	2015/12/25	Deciphered Date	2013/09/01	Title	
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				Size	Document Number
				Custom	LA-K531P
Date:		Tuesday, August 25, 2020		Sheet	70 of 121
				Rev	1.0



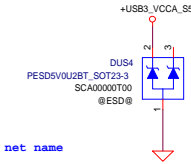
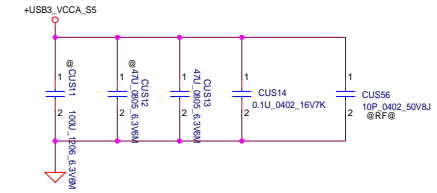
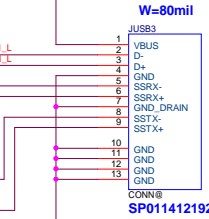
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Issued Date	2015/12/25	Deciphered Date	2016/09/24	Title		
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				Size C	Document Number	Rev
				LA-K531P		
				Date:	Tuesday, August 25, 2020	Sheet 72 of 121



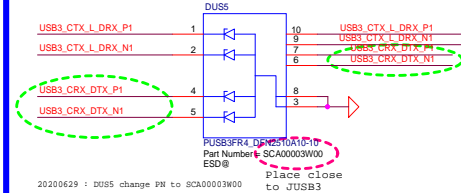
20200415 Remove U3 Redriver



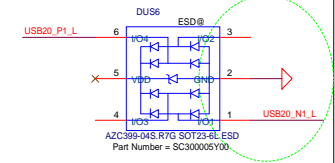
Rear USB3.1 GEN2



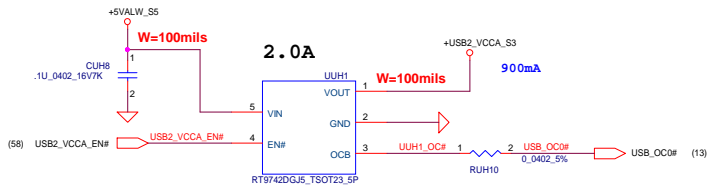
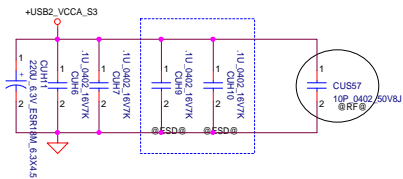
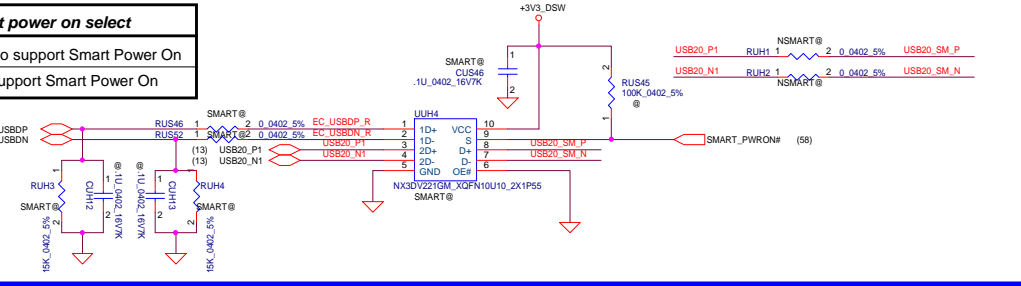
20200416 Correct DUS5 U3 net name



20200413 DUS6 change to SC300005Y00

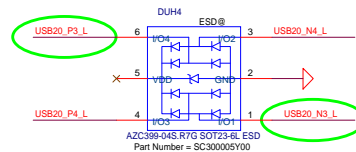


SMART_PWRON#	Smart power on select
H	D = D2 No support Smart Power On
L	D = D1 Support Smart Power On



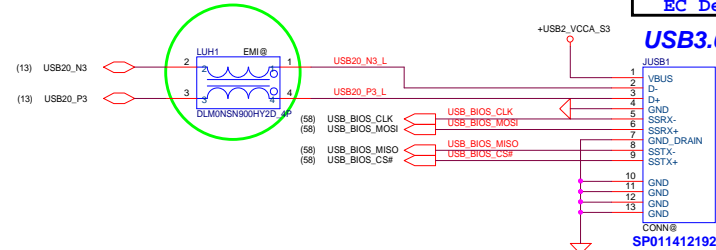
20200424 modify DUH4 Pin define for routing

20200430 swap Pin1/Pin6

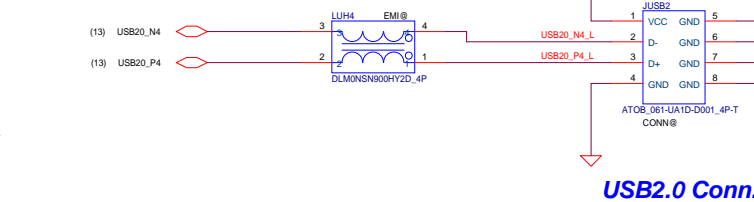
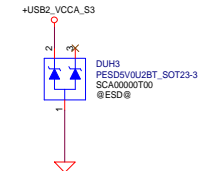
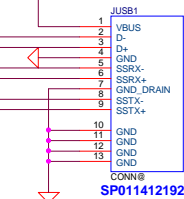


20200413 DUH4 change to SC300005Y00

20200430 LUH1 Swap pin for layout routing

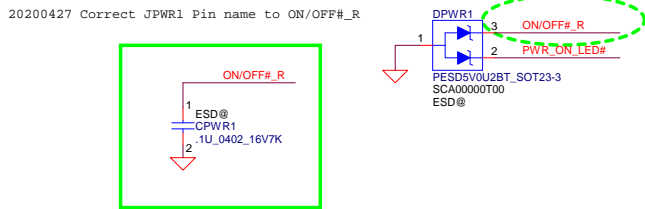
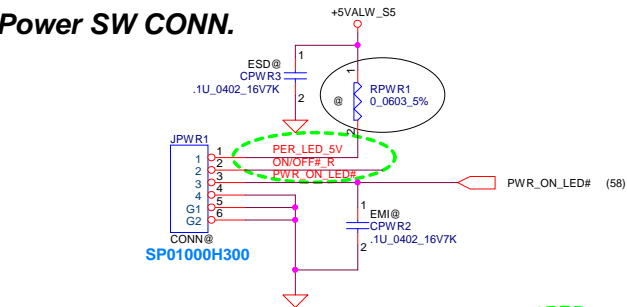


EC Debug Port USB3.0 Conn.



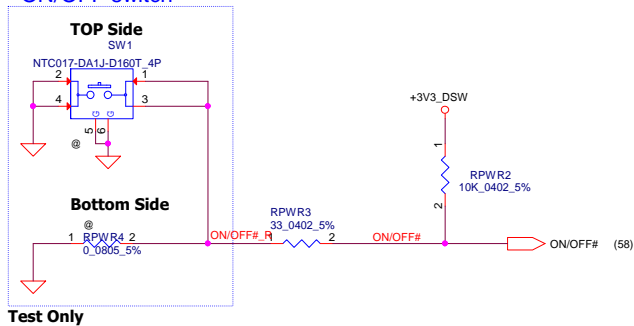
USB2.0 Conn.

Power SW CONN.

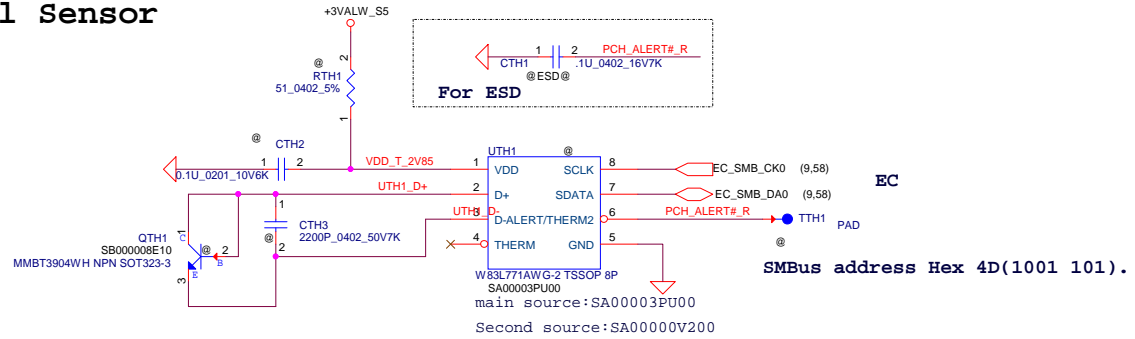


Power Button

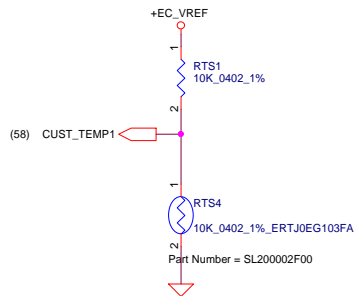
20200807 SW1 -> @
ON/OFF switch



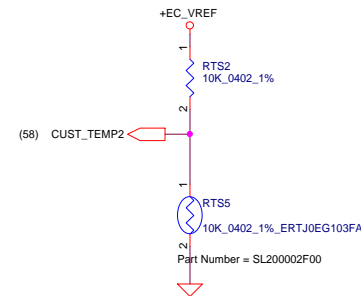
Thermal Sensor



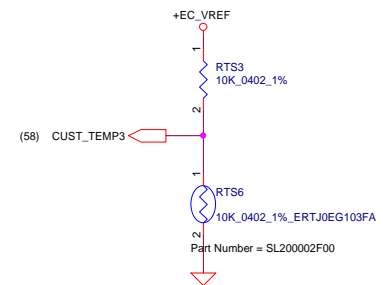
SYSTEM



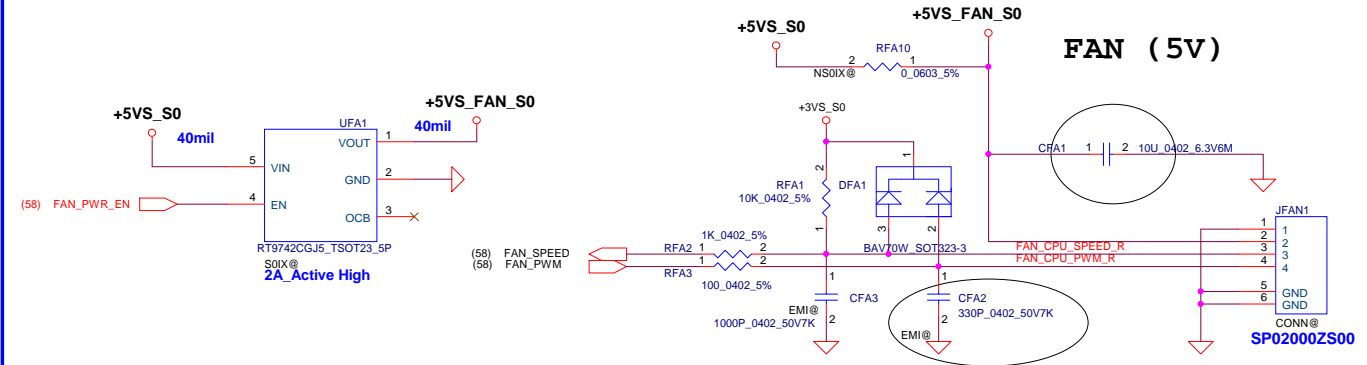
CPU Fan



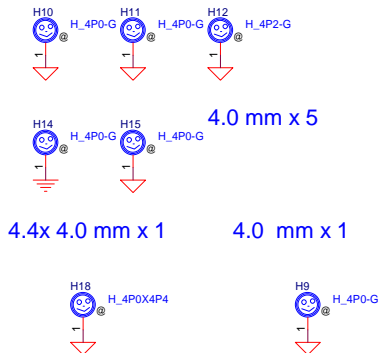
SSD



FAN (5V)



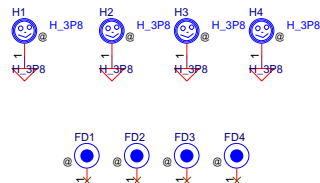
PCB Screw Hole



Stand off Location

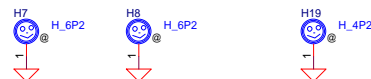
CPU Hole

3.8mm x 4



SSD Hole

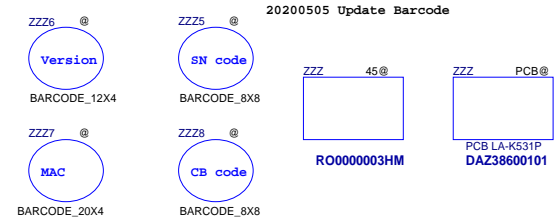
6.2 mm x 2



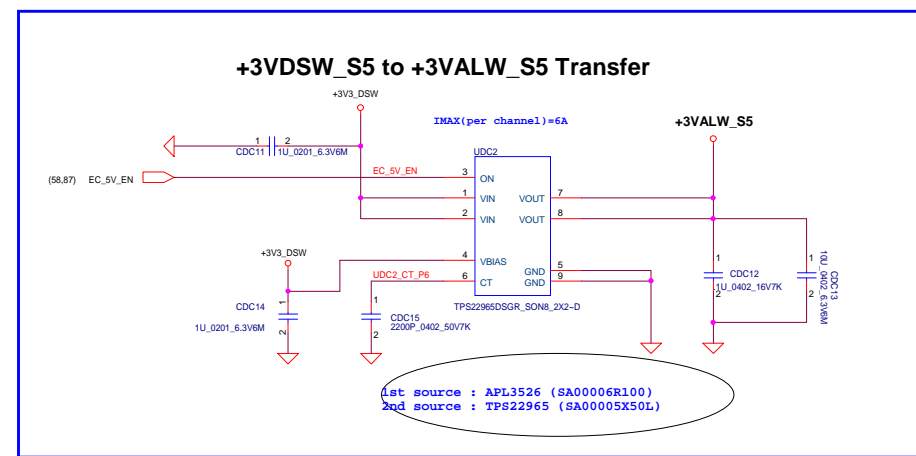
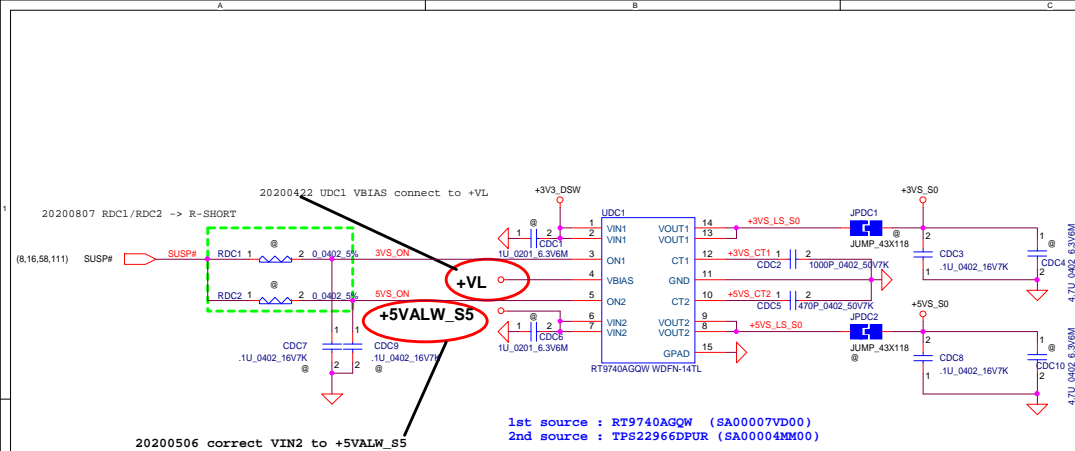
WIFI Hole



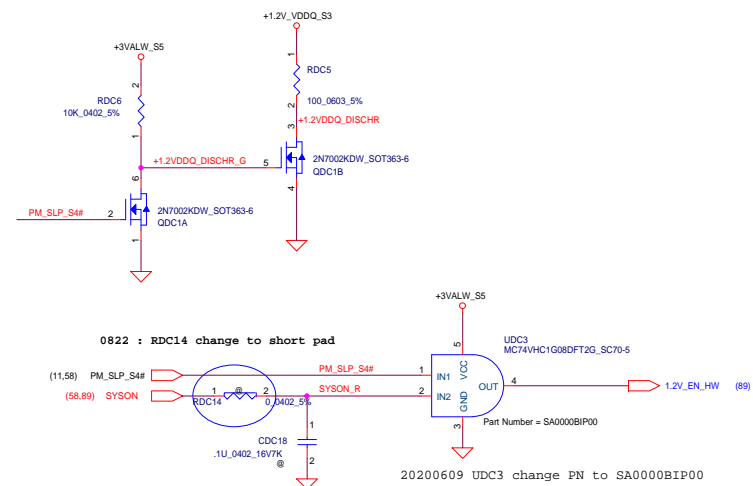
BARCODE



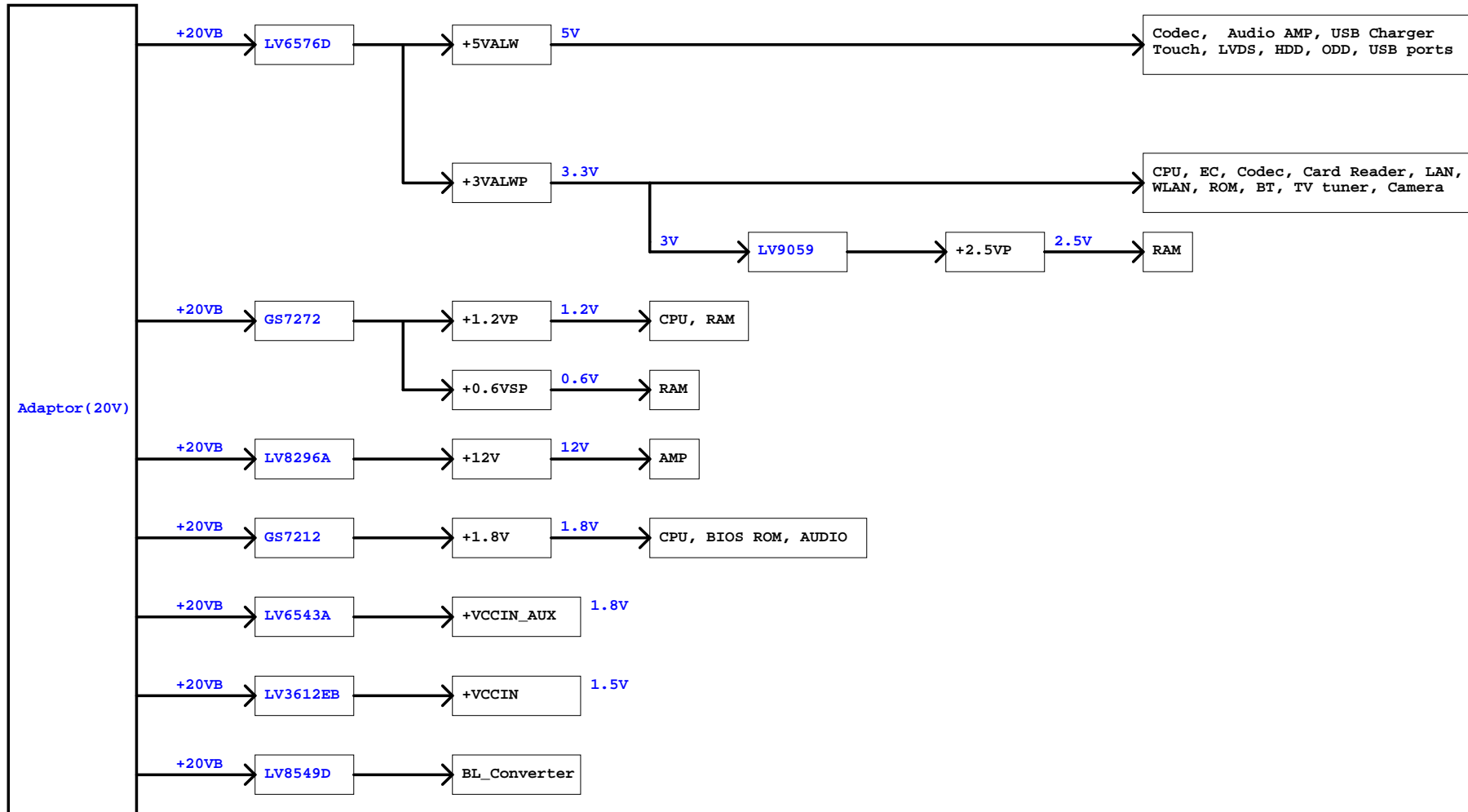
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								Size	Document Number	Rev
								Custom	LA-K531P	0.1
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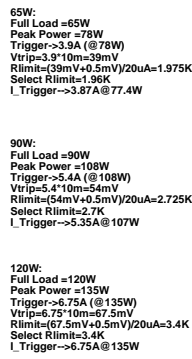


20200409 : Remove QDC2 Circuit

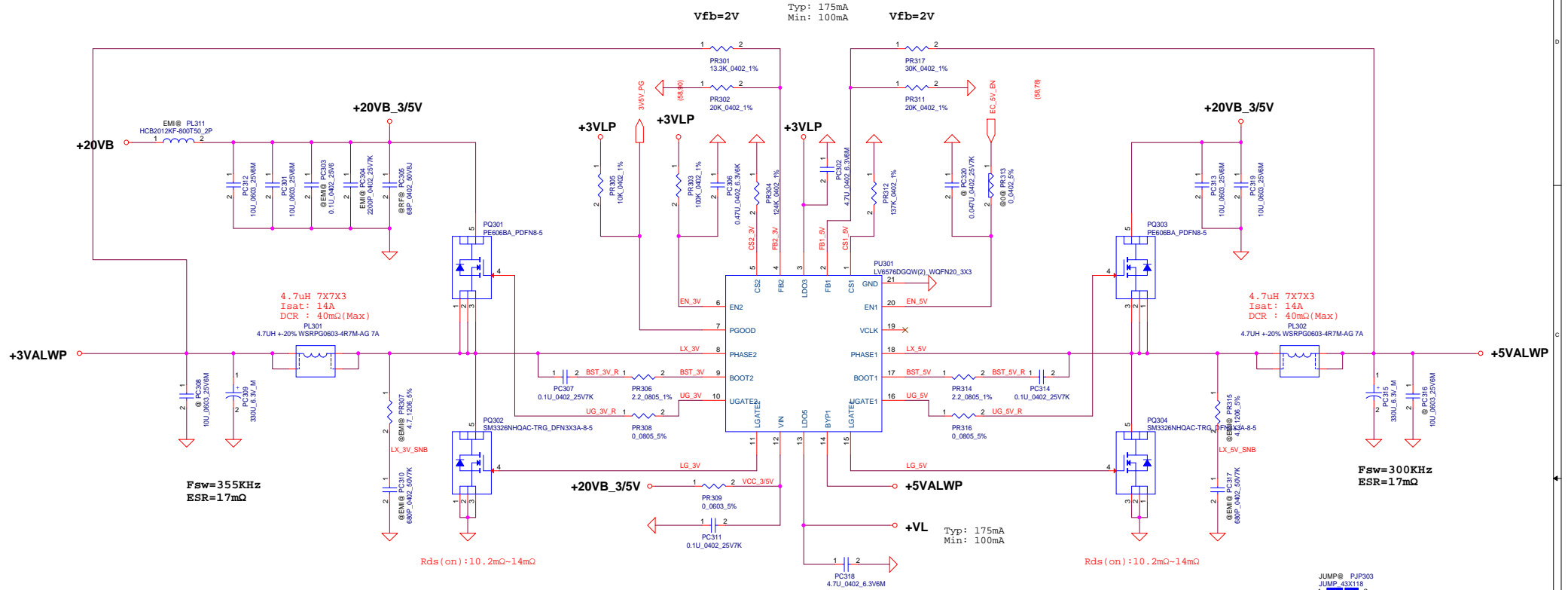


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Size	C	Document Number	LA-K531P	Rev	0.1	
Date:	Tuesday, August 25, 2020	Sheet	78	of	121	



[illegible]

1st source: LV6576D
2nd source: GS7225BTQ-RLV



+3VALWP
Vin = 20V
Iin = $3.3 \times 4.9 / 0.85 / 20$
= 0.95A

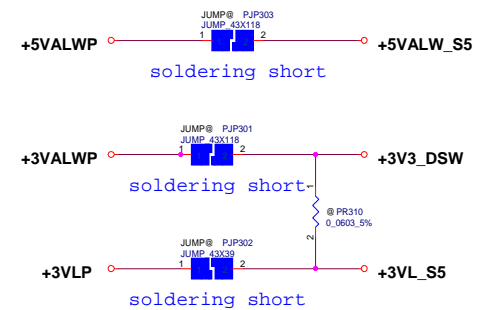
Vout = $V_{fb} \times [1 + (R_t/R_b)]$
= $2 \times [1 + (13.3K/20K)]$
= 3.3V

+3VALWP
Imax=3.4A, Ipeak=4.9A; Fsw=355KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:10.2mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=10~13.5A
Iin_ripple=1.27A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.651A
LIR=Delta IL/Ipeak=0.337
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=193.48uF
CINBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.67uF

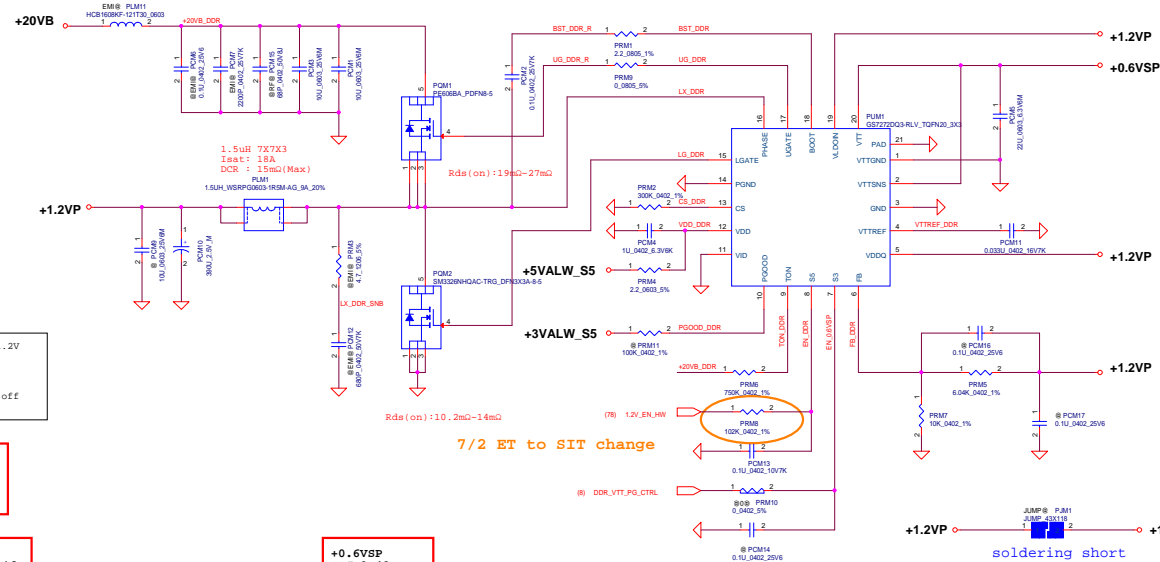
+5VALWP
Vin = 20V
Iin = $5 \times 7.02 / 0.85 / 20$
= 2.07A

Vout = $V_{fb} \times [1 + (R_t/R_b)]$
= $2 \times [1 + (30K/20K)]$
= 5V

+5VALWP
Imax=4.9A, Ipeak=7A; Fsw=300KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:10.2mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=10A~14A
Iin_ripple=2.12A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.66A
LIR=Delta IL/Ipeak=0.38
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=180.6uF
CINBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.53uF



```
1st source: GS7272DQ3-RLV
2nd srouce: LV8231AGQW
```




7/2 ET to SIT change

(5) DDR_VTT_PG_CTRL



A diagram showing a red line representing a wire or solder bridge. The line starts at a red circle on the left labeled '+1.2VP' and ends at a red circle on the right labeled '+1.2V_VDDQ_S3'. In the middle of the line, there are two blue squares representing components, labeled '1' and '2'. Above the squares is the text 'JUMP 431116'. Below the squares is the text 'soldering short'.

+0.6VSP ○ — 1  2 — ○ **+0.6VS_VTT_S0**
soldering short

Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

+1.2VP
 $V_{in} = 20V$
 $I_{in} = 1.203 \cdot 7.5 / 0.85 / 20$
 $= 0.53A$

$$\begin{aligned} V_{out} &= V_{fb} * [1 + (R_t / R_b)] \\ &= 0.75 * [1 + (6.04K / 10K)] \\ &= 1.203V \end{aligned}$$

```

+1.2VP
Imax=5.25A, Ipeak=7.5A ;Fsw=350KHz
Iccp=(Rcsi*Itripp)/(8*RdsOn)
Rds: L/S --> typ:1.2mohm; max:14mohm
Itripp=9-11 uA
Iccp(set)=11.25-15 uA
Iin_tripple=1.25A
Output Cap. ESS=10umohm
Delta IL=(Vin-Vo)/L/*(Vout/Vin)*Tj=2.212A
IL=Delta IL/Iccp=0.295
Coat=[L*Idc/Iccp*Delta IL/2]/((Vout+Delta V)*2-Vout*2)
CINBU=Load*Vout*(Vin-Vout)/(Fsw*(Vin*2+VINP)*0.44uF

```

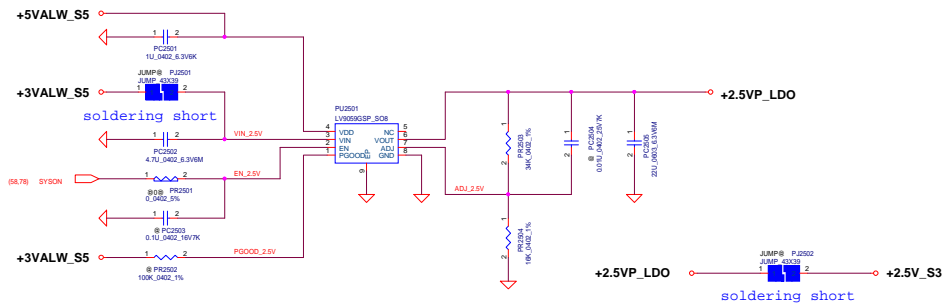
+0.6VSP
TDC=0.42A
Ipeak=0.6A

LV8231A:
Quiescent Current (GND Current)
IQ(typ)=0.135mA
PD(MAX) = (TJ(MAX) - TA) / θ JA=3.33W
 θ JA= 30°C/W

GS7272:
Quiescent Current (GND Current)
IQ(typ)=0.4mA
PD(MAX) = (TJ(MAX) - TA) / θ_{JA} =1.667W
 θ_{JA} = 60°C/W

	main	2nd	
V _o	0.6	0.6	V
V _{in}	1.2	1.2	V
I _o	0.6	0.6	A
PD	3.33	3.33	W
θ _{JA}	30	60	°C/W

1st source: LV9059
2nd srouce: GS7166SO-R
3rd srouce: APL5933CKAI


$$\begin{aligned} V_{out} &= V_{fb} * [1 + (R_t / R_b)] \\ &= 0.8 * [1 + (34K / 16K)] \\ &= 2.5V \end{aligned}$$

+2.5VP
I_{max}=0.35, I_{peak}=0.5A ;
Current Limit=3.6A(Typ)~4.2A(Max)

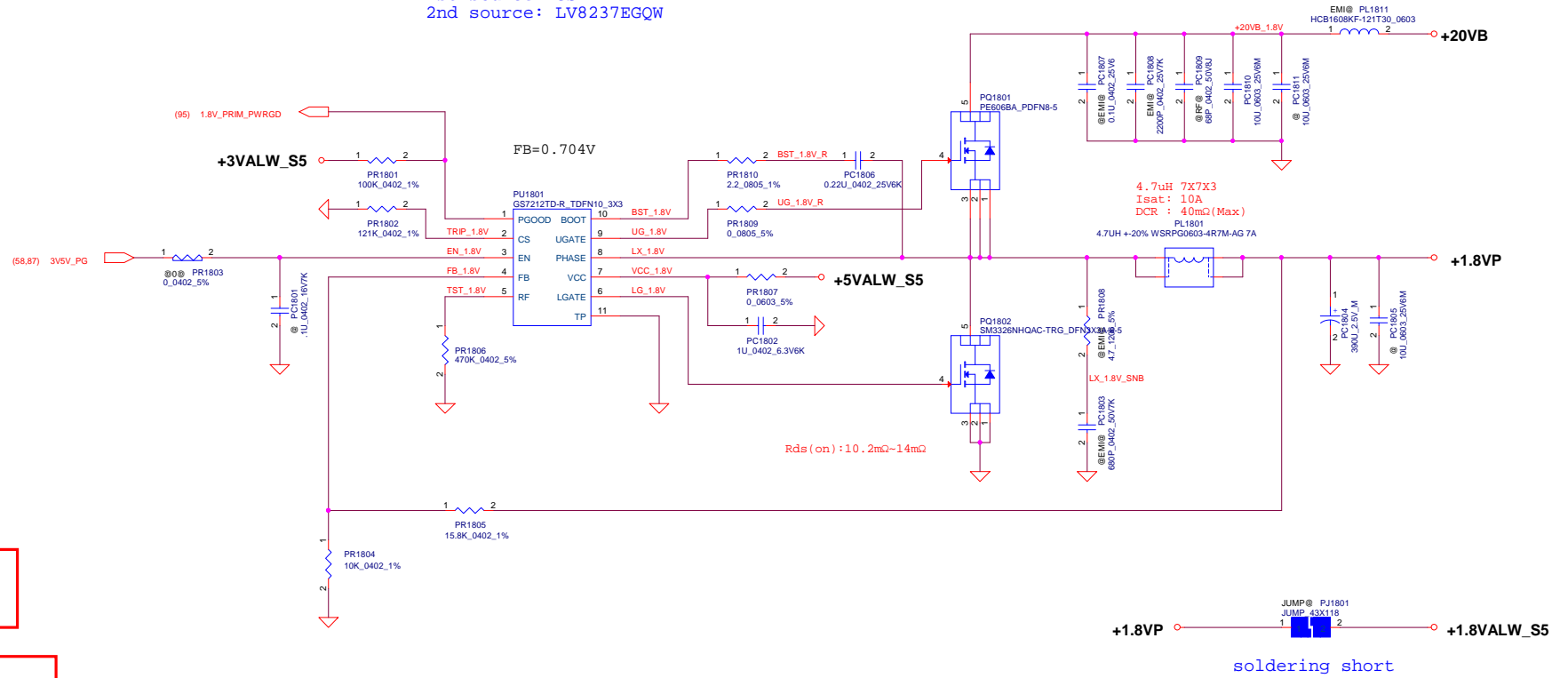
LV9059:
Quiescent Current (GND Current)
IQ(typ)=0.6mA
 $PD(MAX) = (TJ(MAX) - TA) / \theta JA = 2.96W$
 $\theta JA = 33.7^{\circ}C/W$

APL5933CKAI:
Quiescent Current (GND Current)
IQ(typ)=1mA
PD(MAX) = (TJ(MAX) - TA) / θ_{JA} = 2W
 θ_{JA} = 50°C/W

GS7166:
Quiescent Current (GND Current)
IQ(typ)=1mA
 $PD(MAX) = (TJ(MAX) - TA) / \theta JA = 1.33W$
 $\theta JA = 75^{\circ}C/W$

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			Date	Issued
			Ym	Mo
			Day	Year
			Model	Rev
			Ver	Rev

1st source: GS7212TD-R
2nd source: LV8237EGQW



+1.8VP
Vin = 20V
Iin = 1.816*3.5/0.85/20
= 0.374A

Vout = Vfb*[1+(Rt/Rb)]
= 0.704*[1+(15.8K/10K)]
= 1.816V

+1.8VP
Imax=2.45A, Ipeak=3.5A ; Fsw=290KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:10.2ohm ; max: 14mohm
Itrip=9-11 uA
Iocp(set)=10A-14A
Iin_ripple=0.7A
Output Cap. ESR=10mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.202A
LIR=Delta IL/Ipeak=0.343
Cout=[L*(Iout+Delta IL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=165.47uF
CINBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.35uF

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				0.1
				Date
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Module model information
RT6543A_V1A.mdd for IC portion
RT6543A_V1B.mdd for SW portion
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OCP is Lowside MOSFET Rdson sense

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226K x1.2
255K x1.4
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6/11 ET to SIT change

7/27 SIT to SVT change 8/1/2017

High > 1V
Low <0.4V

+3VALW
V_PRIM_PWRGD

(90) 1.8V_PRIM_PWRGD

(11,17) VID1_AUX

+5V AI W S5

6/15 ET to SIT change

+3VALW_S5

VCCIN_AUX VID Follow Intel PDG Rev0.71

VID1	VID0	+VCCIN_AUX
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

+VCCIN_AUX
TDC 14A(1H1L)
Peak current 32A
OCP current 45A
LL=1mohm

FSW=400kHz
DCR 0.98mohm +/-5%

0.22uH 7X7X4
Isat : 50A
DCR : 0.98±5%

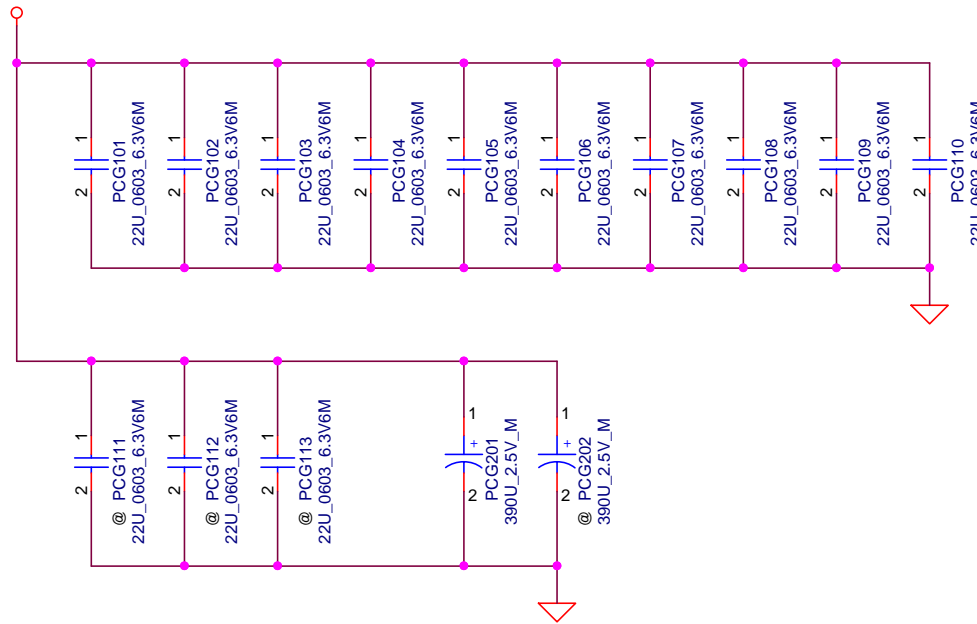
PLG1
S COIL 0.22UH W/SRPG0604-R22M-AG-R98 35A

VCCIN ALIX

B=3435 (B25/85)

6/11 ET to SIT change

+VCCIN_AUX



VCCIN_AUX (ET)

22uF_0603 13 pcs (test :8 pcs)
390uF_10m 1 pcs

VCCIN_AUX (SIT)

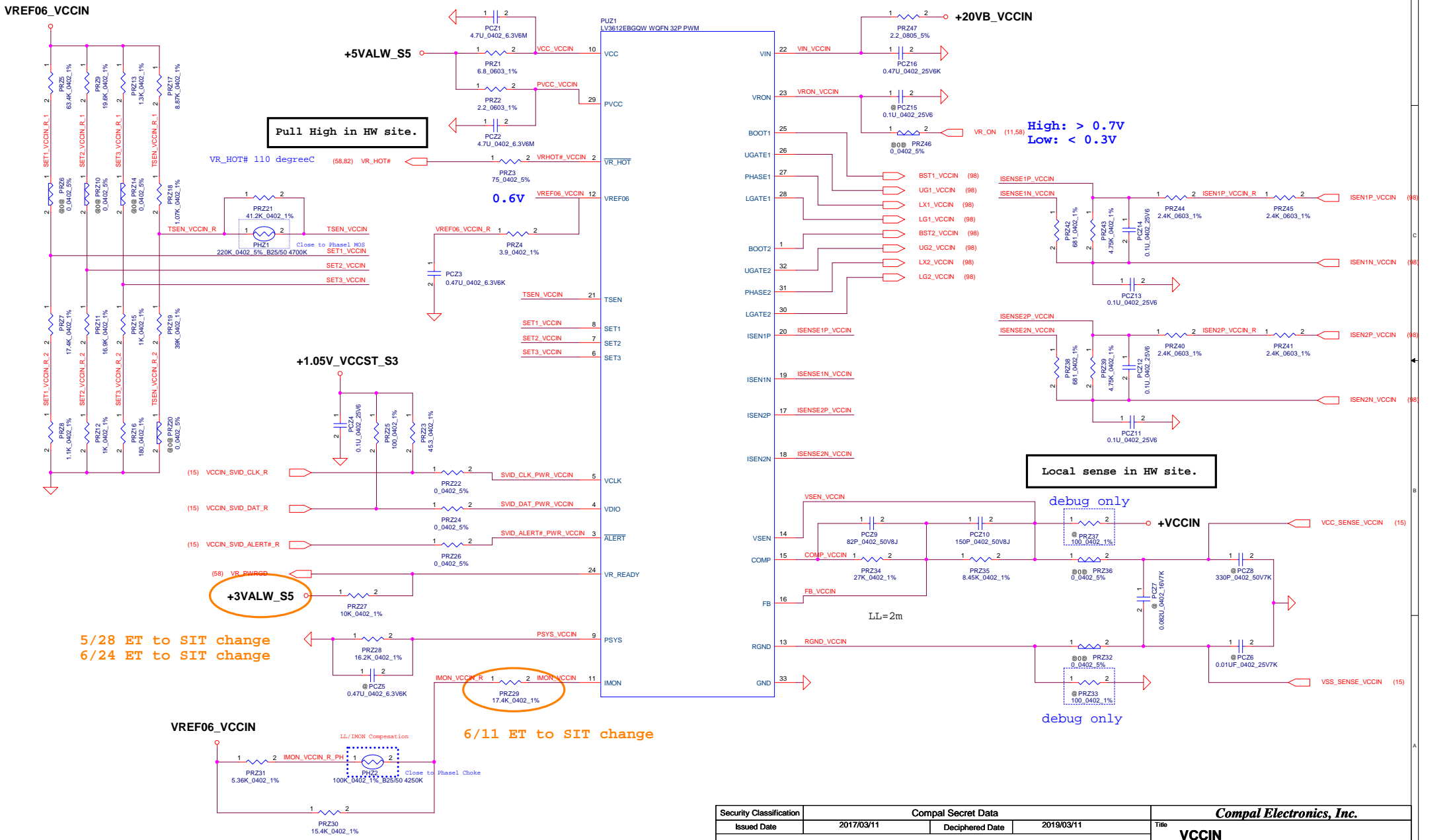
22uF_0603 8 pcs
390uF_10m 1 pcs

VCCIN_AUX (SVT)

22uF_0603 10 pcs
390uF_10m 1 pcs

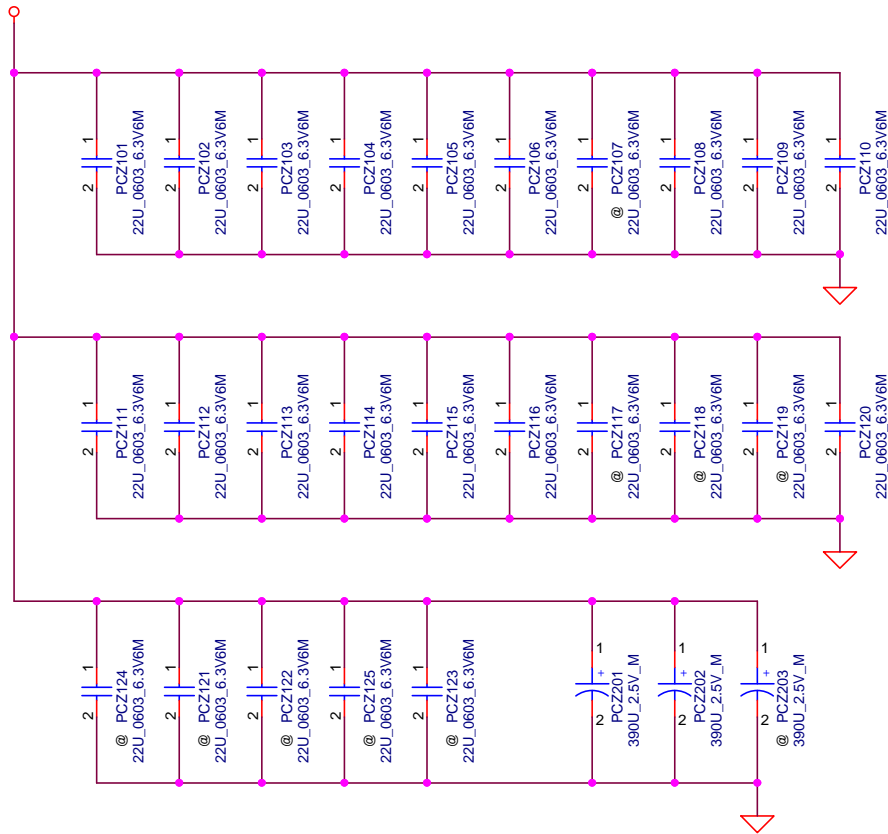
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Module model information
RT3612EB_2Phase_V1A.mdd for IC portion
RT3612EB_2Phase_V1B.mdd for SW portion



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+VCCIN



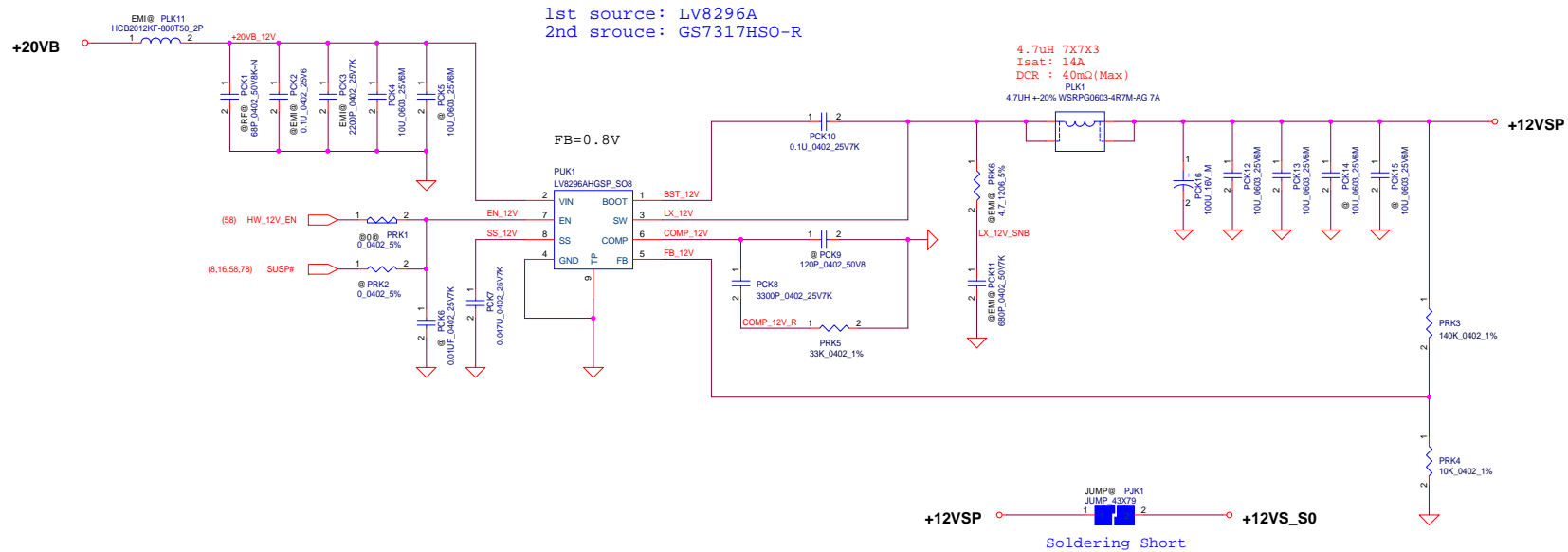
VCCIN (ET)

22uF_0603 20 pcs (test : 16pcs)
390uF_10m 2 pcs

VCCIN (SIT)

22uF_0603 16 pcs
390uF_10m 2 pcs

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+12VSP
 $V_{in} = 20V$
 $I_{in} = 12 \times 0.83 / 0.85 / 20$
 $= 0.94A$

$V_{out} = V_{fb} \times [1 + (R_t / R_b)]$
 $= 0.8 \times [1 + (140K / 10K)]$
 $= 12V$

+12VSP
 $I_{max} = 0.93A$, $I_{peak} = 1.33A$, $F_{sw} = 340KHz$
 Current Limit = 3.8A (Min) ~ 6.4A (Max)
 $I_{in_ripple} = 0.86A$
 $\Delta I_L = [(V_{in} - V_o) / L] \times [(V_{out} / V_{in}) \times T] = 3.004A$
 $LIR = \Delta I_L / I_{peak} = 2.253$
 $C_{out} = [L \times (I_{out} + \Delta I_L / 2) \times 2] / [(V_{out} + \Delta V)^2 - V_{out}^2]$
 $= 4.79uF$
 $CINBULK = I_{Load} \times V_{out} \times (V_{in} - V_{out}) / (F_{sw} \times V_{in}^2 \times VINPP) = 0.33uF$

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